JST – DFG Joint Workshop

January 21, 2009

Atomic level material processing and characterization for nanoscale CMOS transistors

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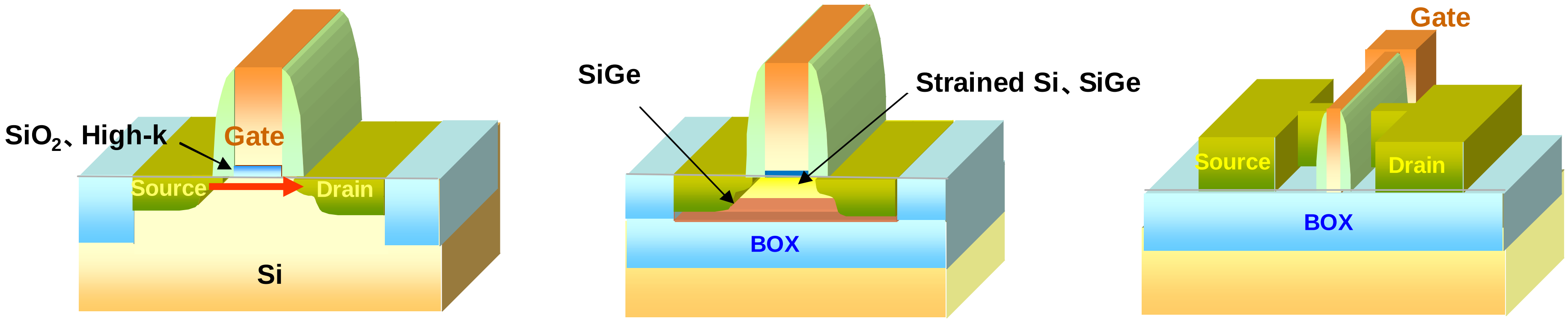
MIRAI project

New Materials and Structures for Ultra-scaled MOSFET

Structure evolution for gate control



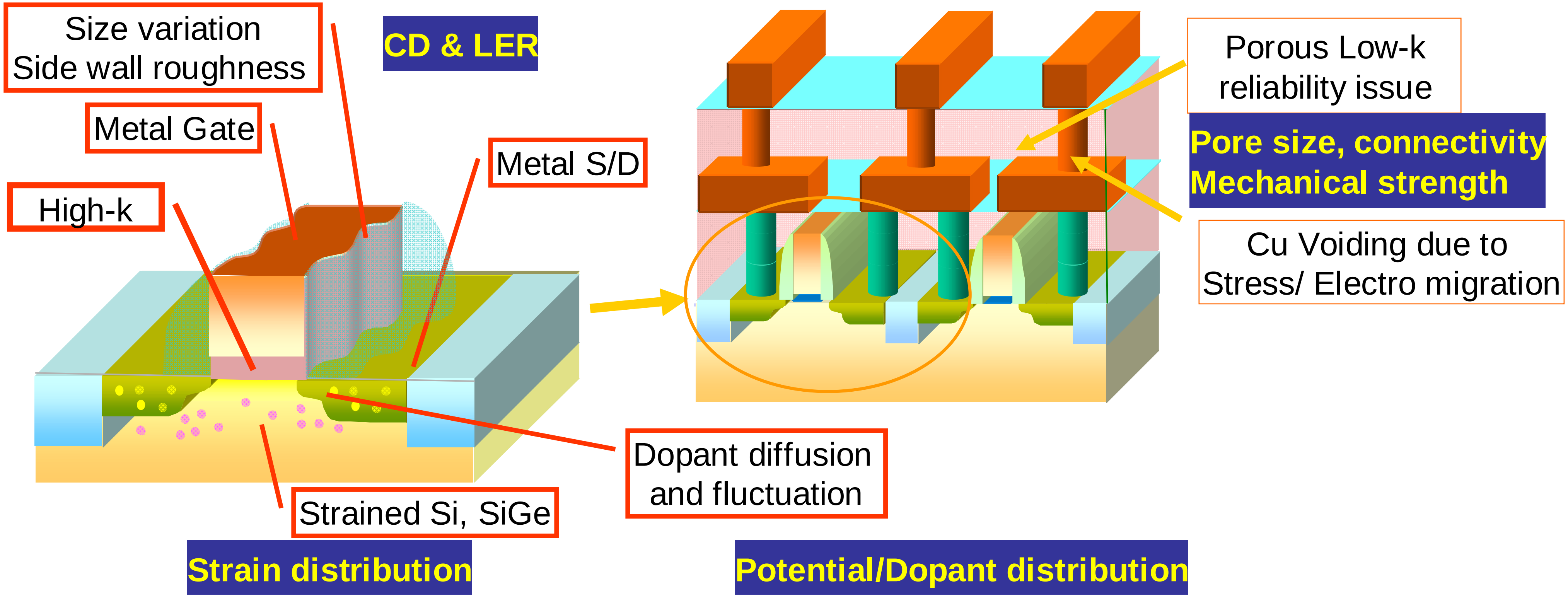
Planar FET　　Strained SOI、SGOI FET　　Multi-gate FET

Materials evolution for high drive current

	Present		Future
Channel	Si	→	High-mobility Materials (Strained Si, SiGe, Ge)
Gate Dielectrics	SiO_2 (SiON)	→	High-k Dielectrics (HfSiO, HfAlO, LaAlO)
Gate Electrode	Poly-Si	→	Metal, Metal Silicide
Source/Drain	Si	→	SiGe, SiC, MSi_x, MGe_x

Keeping Ioff low and enhancing Ion by optimal selection of materials and structures

Increasing Requirements for Metrology and Characterization Technology



Major Issues

- **Technology boosters, i.e., new materials/structures and processes are rushing into semiconductor technology.**
- **Variability increases.**

To implement new technologies while minimizing variation,
reliable characterization and metrology technologies are crucially needed.

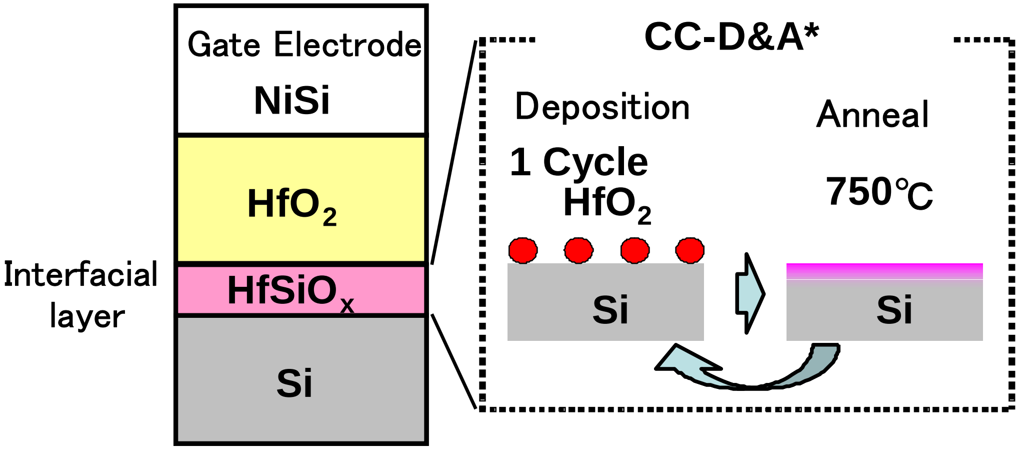
Contents

For the fabrication of Nano CMOS Transistors

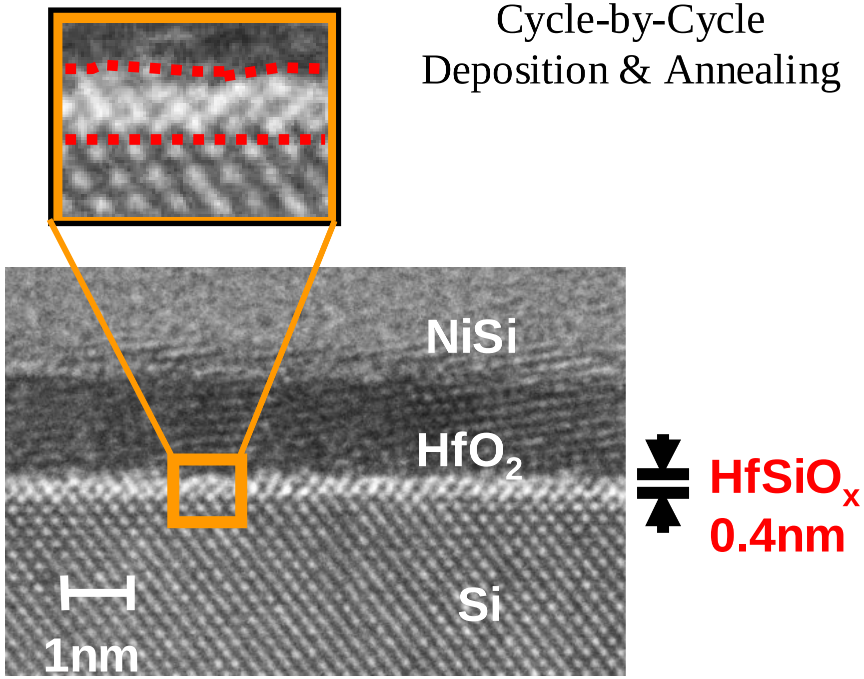
What do we need?

- Gate stack (Gate dielectrics and electrode)
- Channel
- Source/Drain

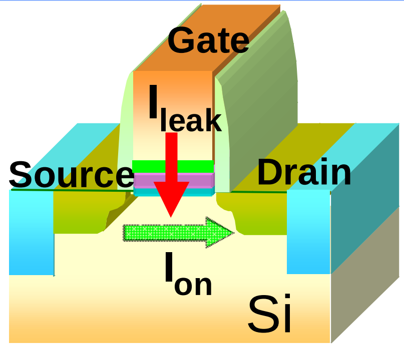
Towards EOT (equivalent oxide thickness) =0.5nm

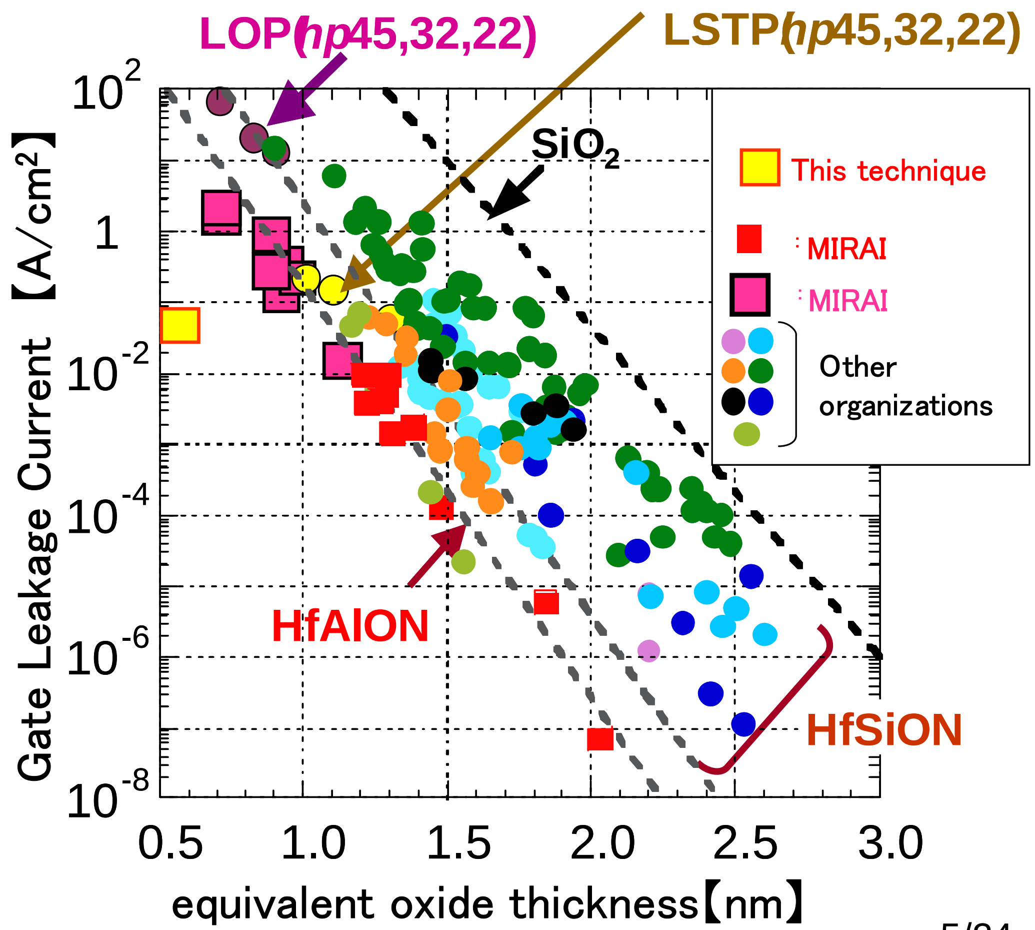


Cycle-by-Cycle
Deposition & Annealing

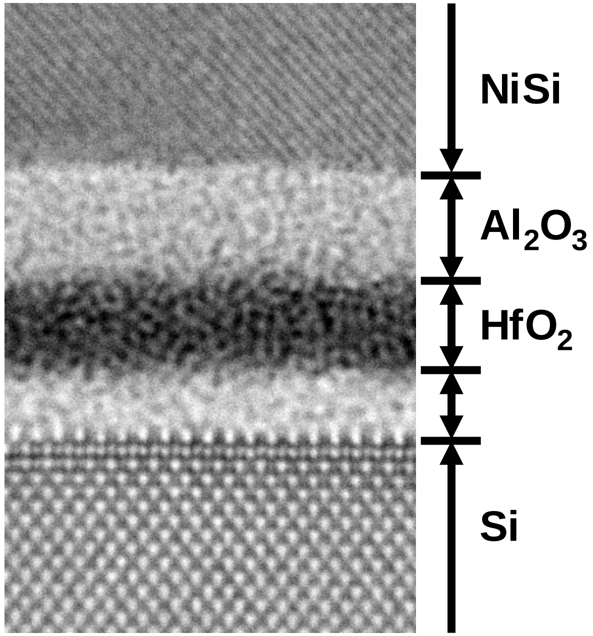


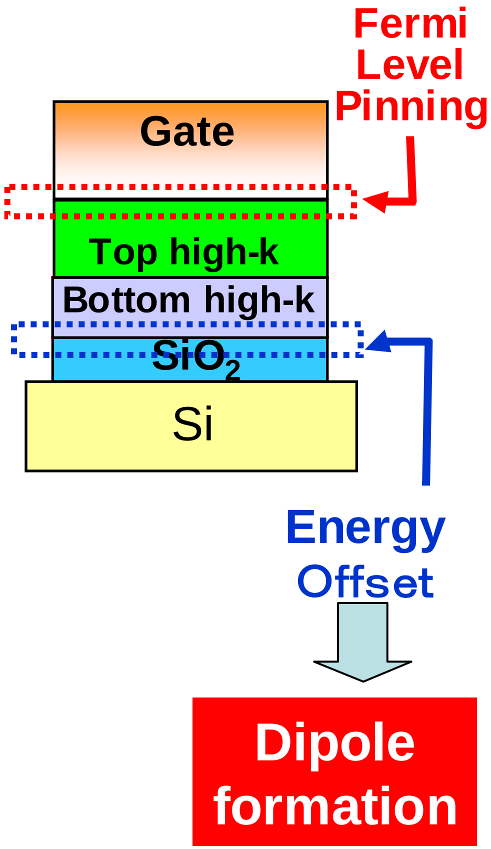
A. Ogawa et al., INFOS (2007)

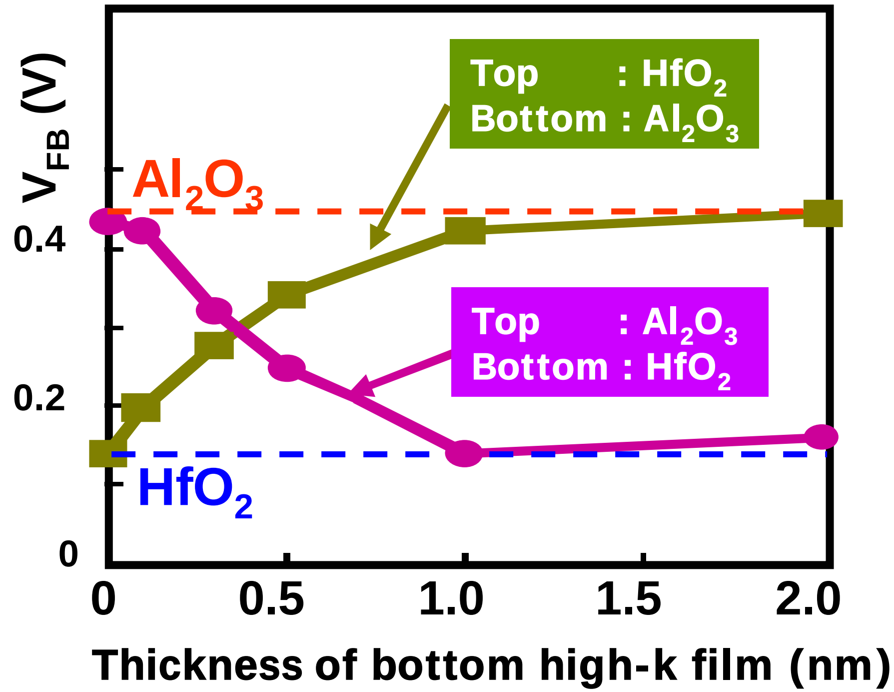




Control of threshold voltage







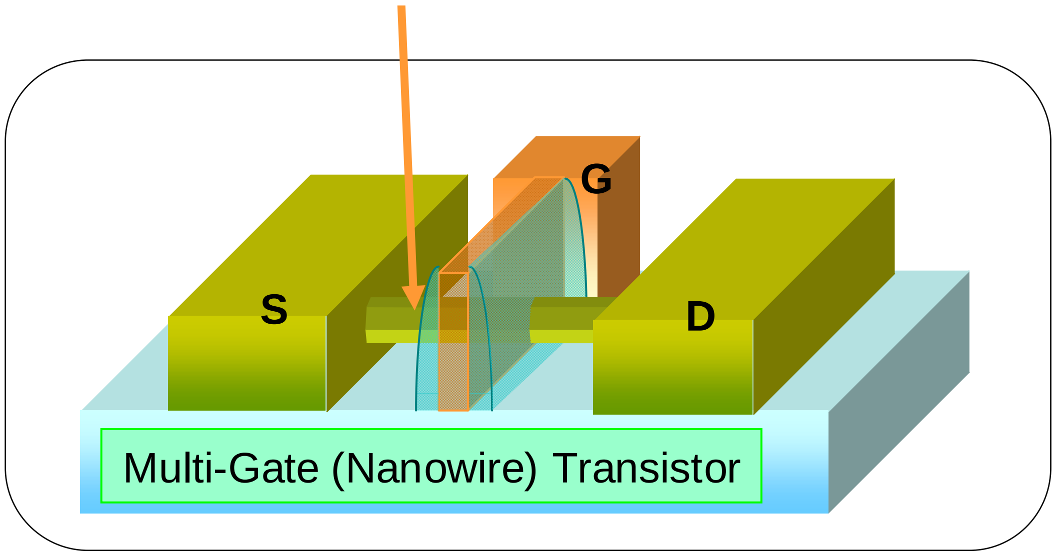
Iwamoto, VLSI Symp. 2007

Contents

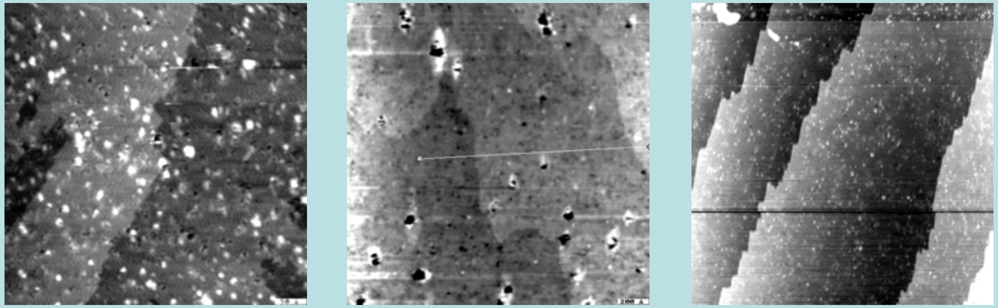
For the fabrication of Nano CMOS Transistors

What do we need?

- Gate stack (Gate dielectrics and electrode)
- Channel: Surface flatness

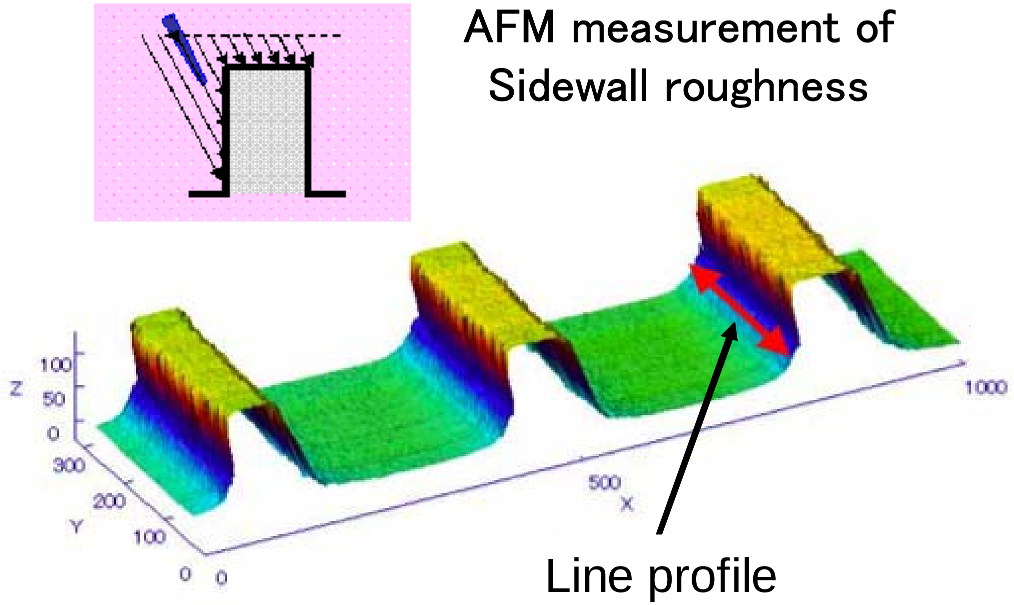


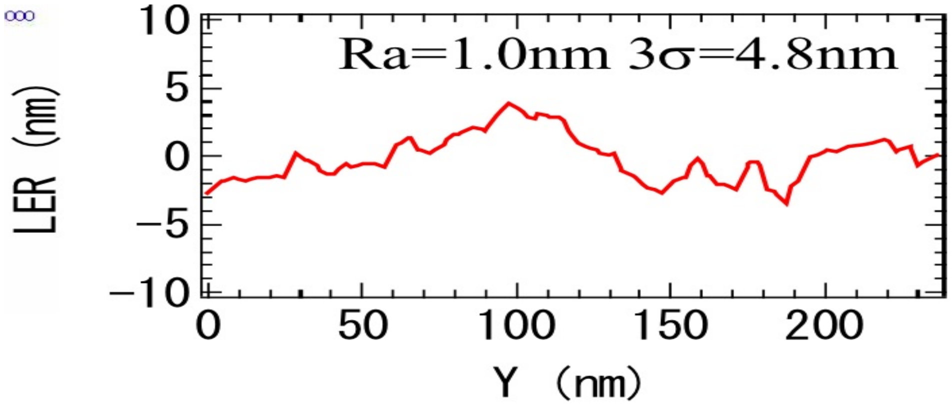
Atomically flattening of Si surfaces



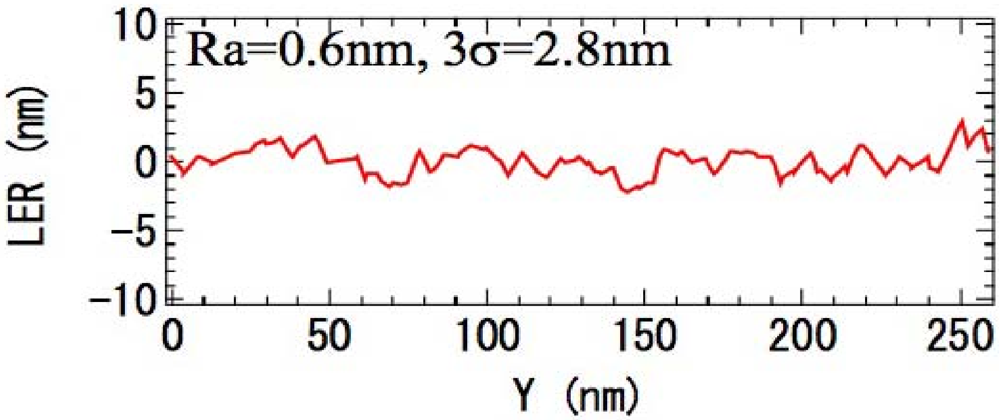
Si(001) Si(110) 200nm□ Si(111)

Low pH HF treatment + Hydrogen anneal（800℃）





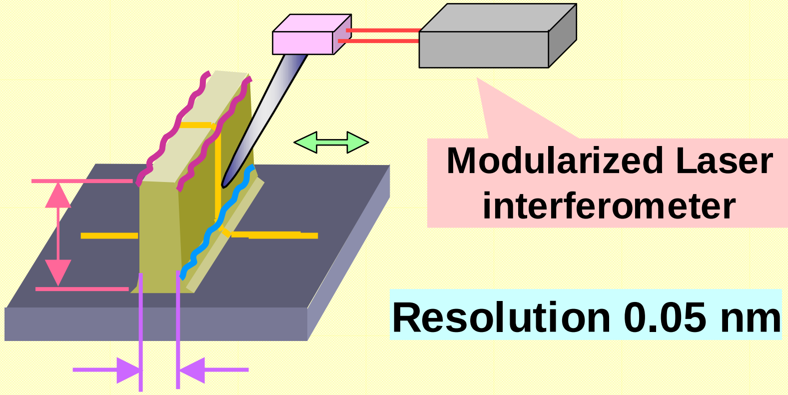
Before H_2 anneal （after RIE）



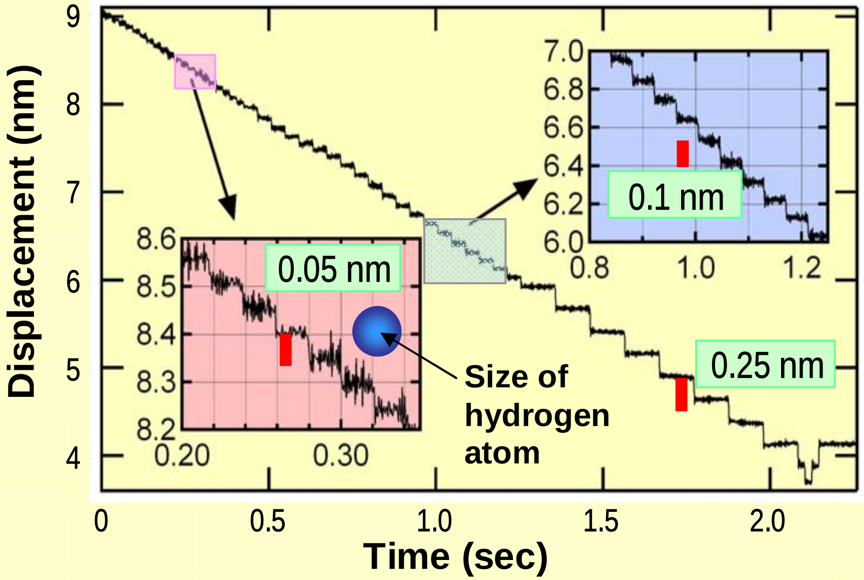
H_2 annealed：800℃, 0.1 torr, 40 s
(SPM + RCA+ LPH + H_2 anneal)

Atomic Precision CD Metrology by AFM

CD-AFM with Laser interferometer

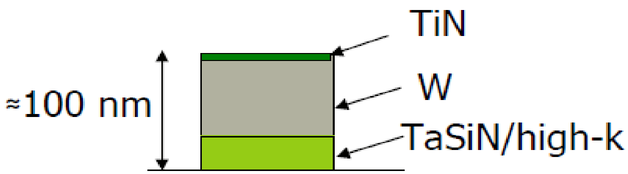


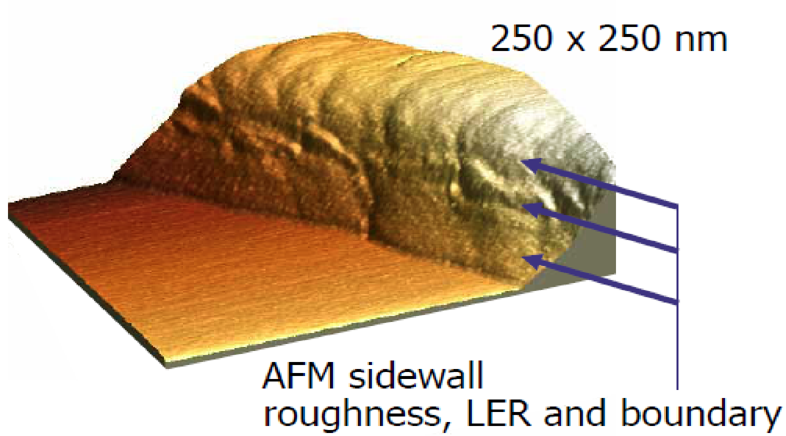
- 3D AFM scanner: parallel spring mechanism.
- Laser interferometer: DSP-based processing.

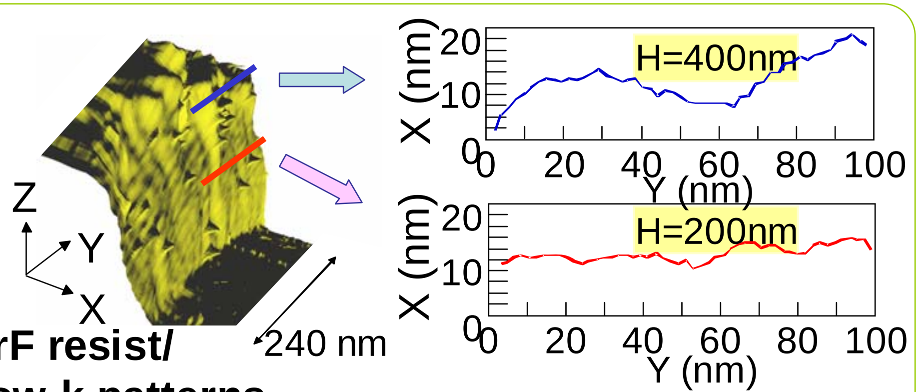


S. Gonda et al., Characterization and Metrology for ULSI Tech., 2005

Sidewall and line edge roughness measured by tilt-step-in operation



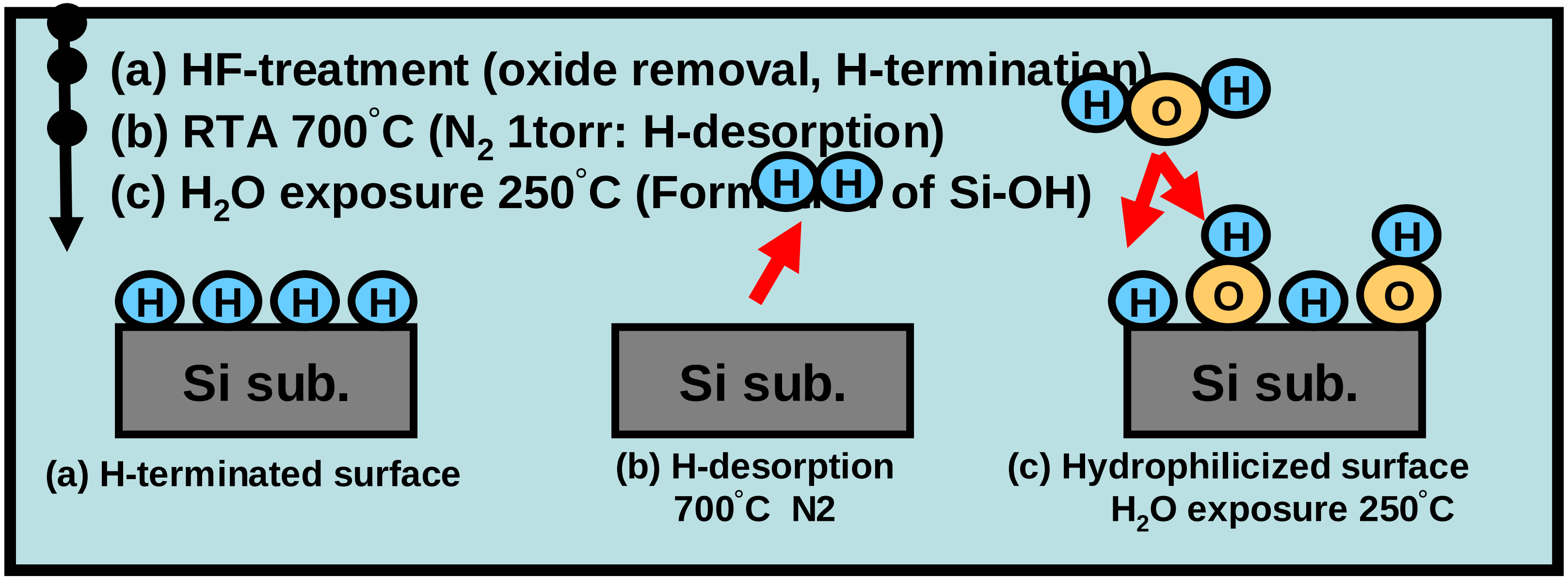


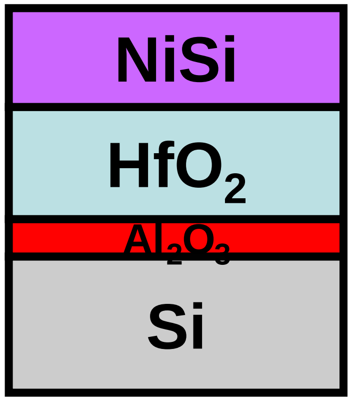


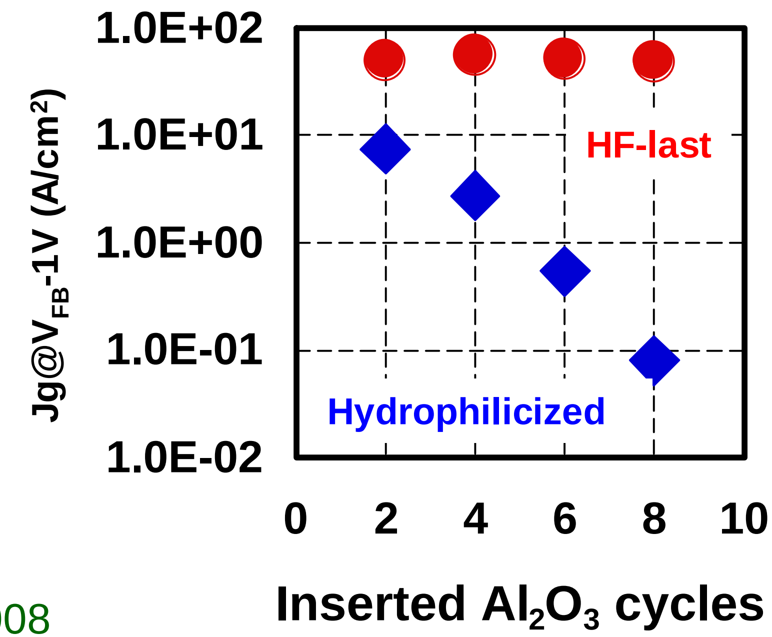
ArF resist/ Low-k patterns

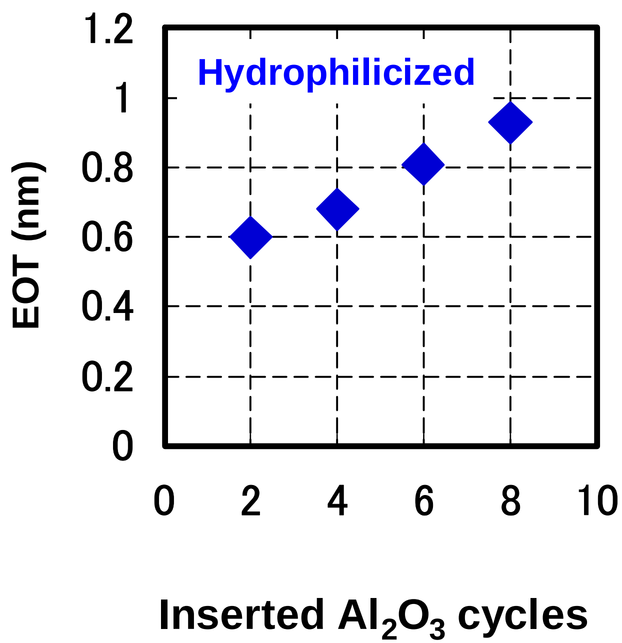
K. Murayama et al, SPIE, 2006

Surface hydrophilicization





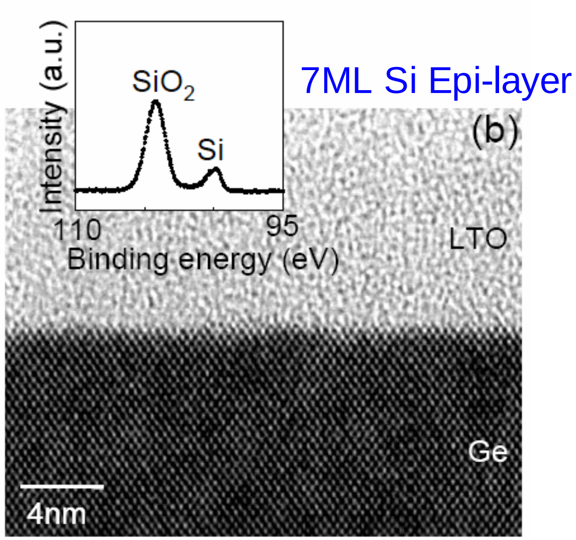


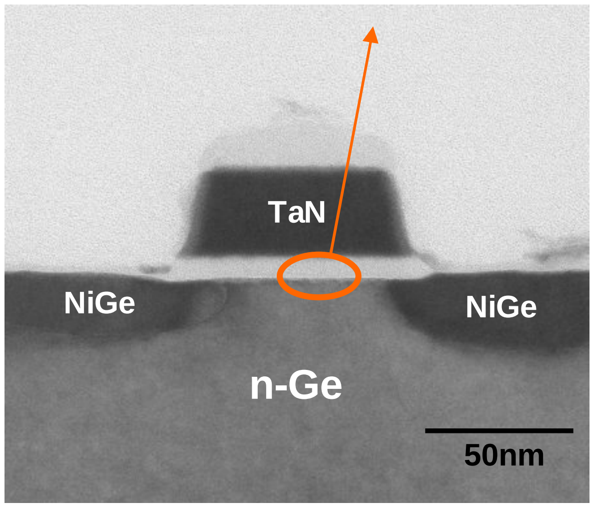


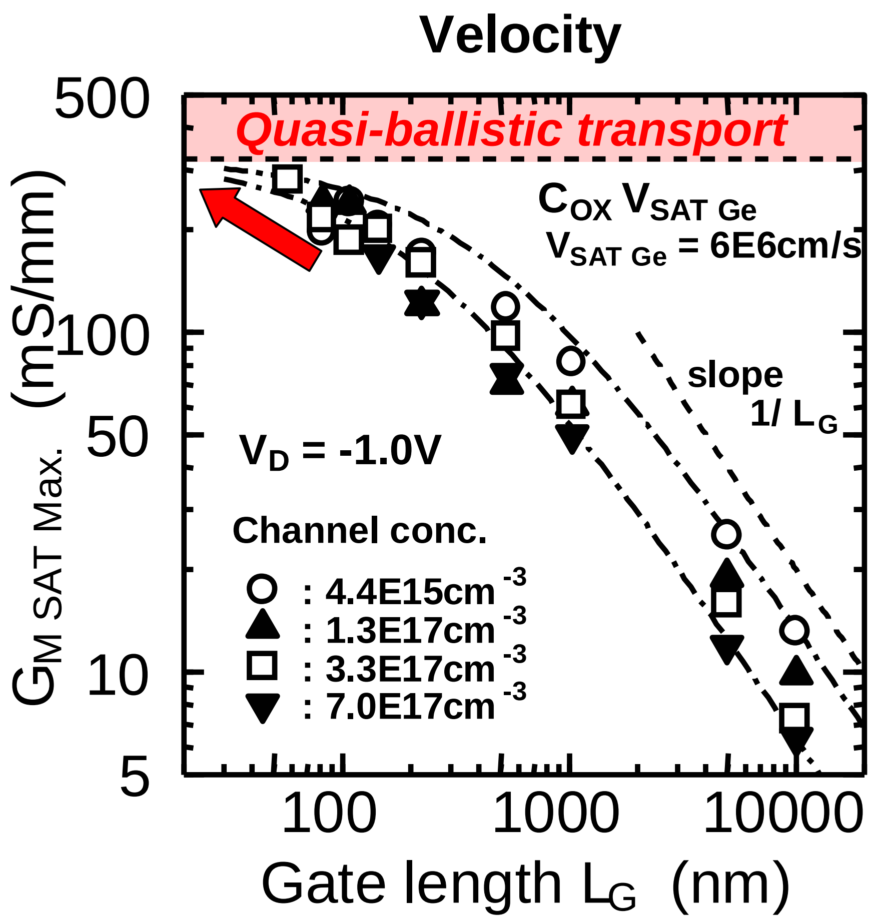
Morita, SSDM 2008

Ge-pMOSFET with Lg=60nm

Si passivation for Gate stack, NiGe Metal S/D





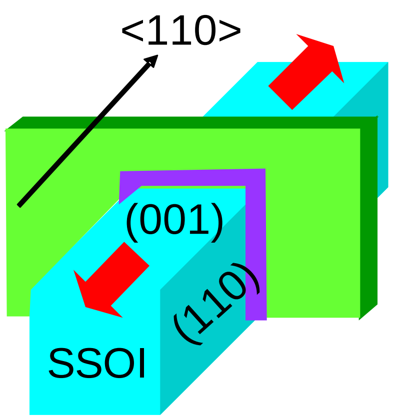


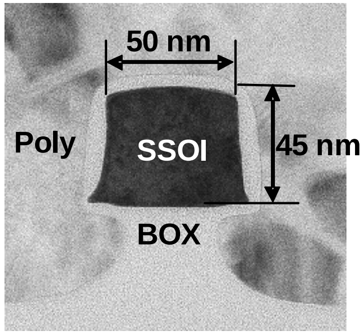
Yamamoto et al. IEDM, 2007

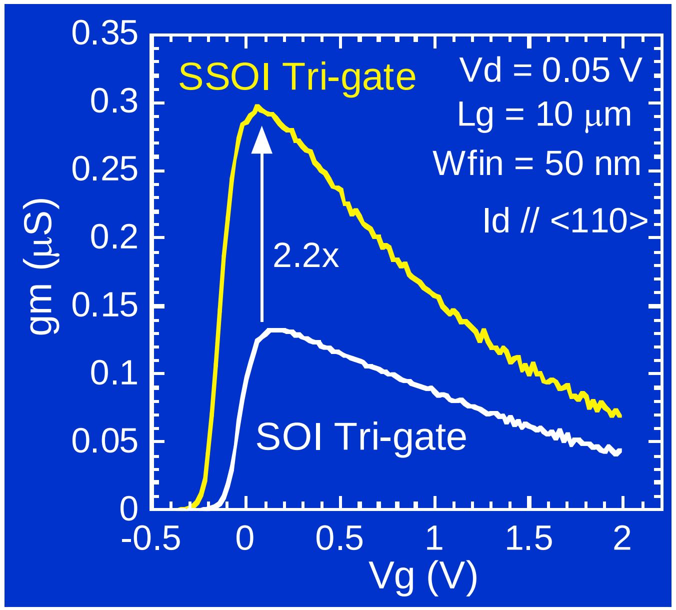
Uni-axially Strained Multi-Gate CMOS Transistors

nMOSFET

Uni-axial tensile strain on Si (110) surface



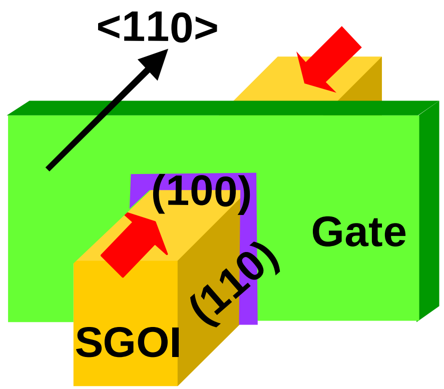


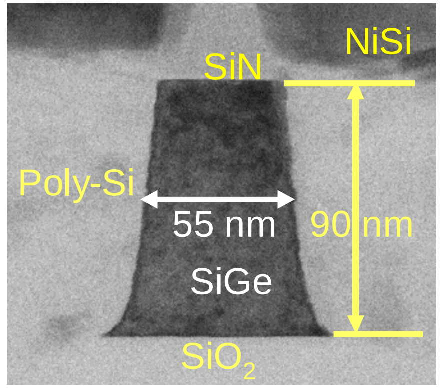


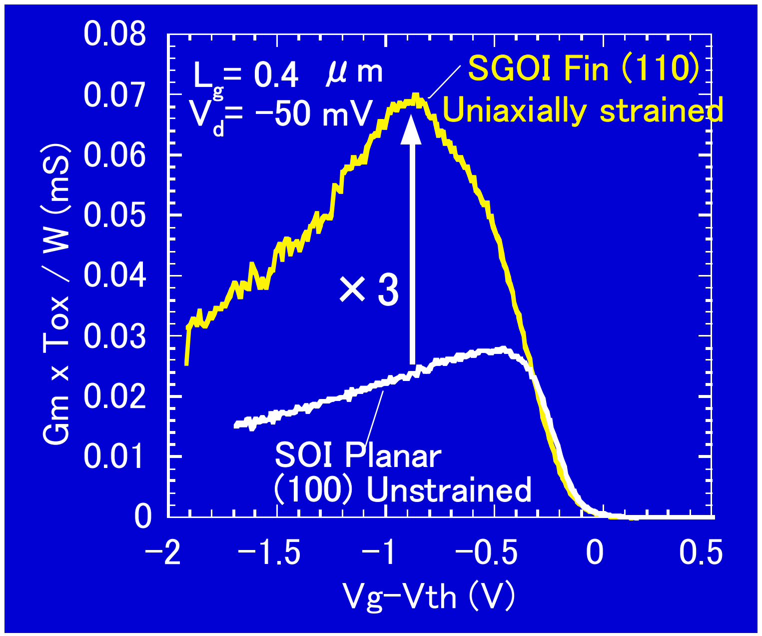
T. Irisawa et al. IEDM, 2006

pMOSFET

Uni-axial Compressive strain on SiGe (110) surface

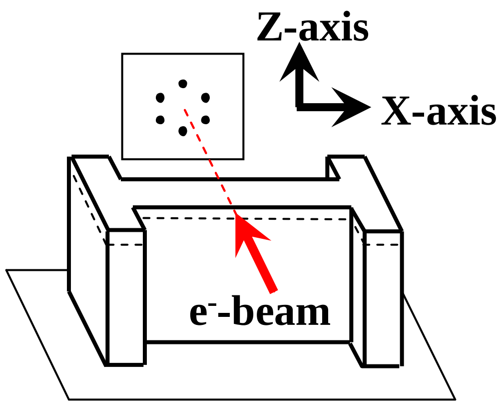


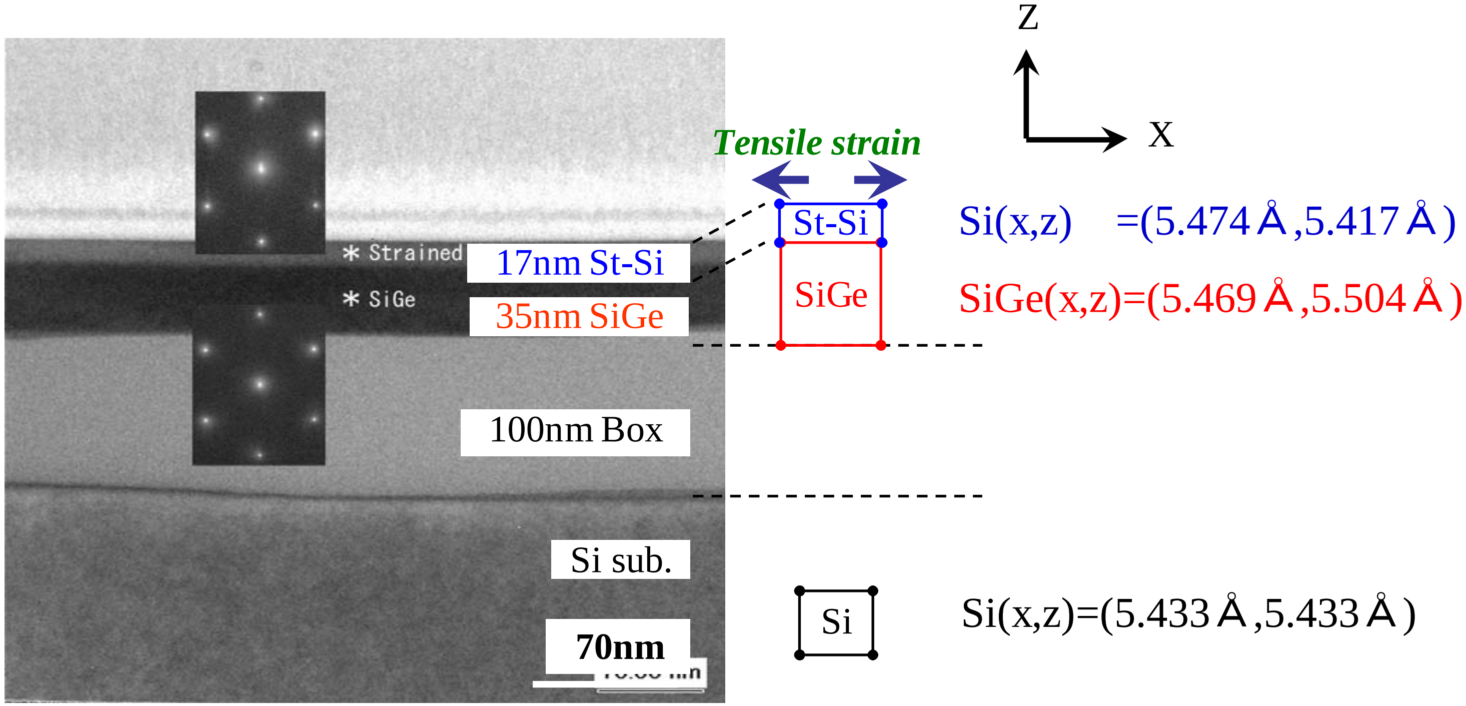




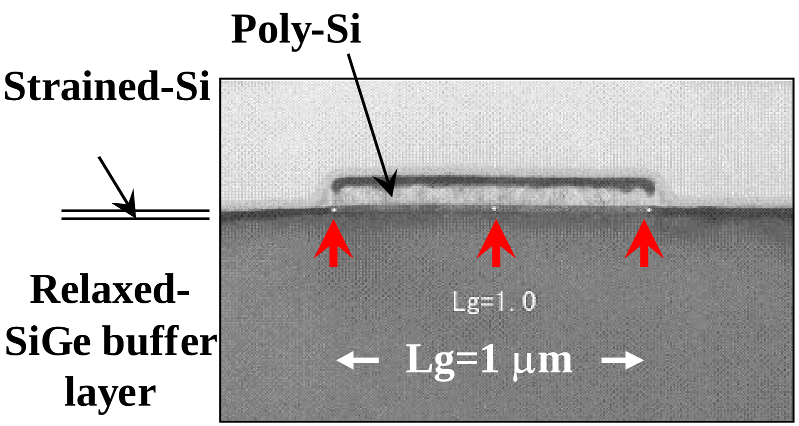
T. Irisawa et al., IEDM, 2005

NBD (NanoBeam electron Diffraction)

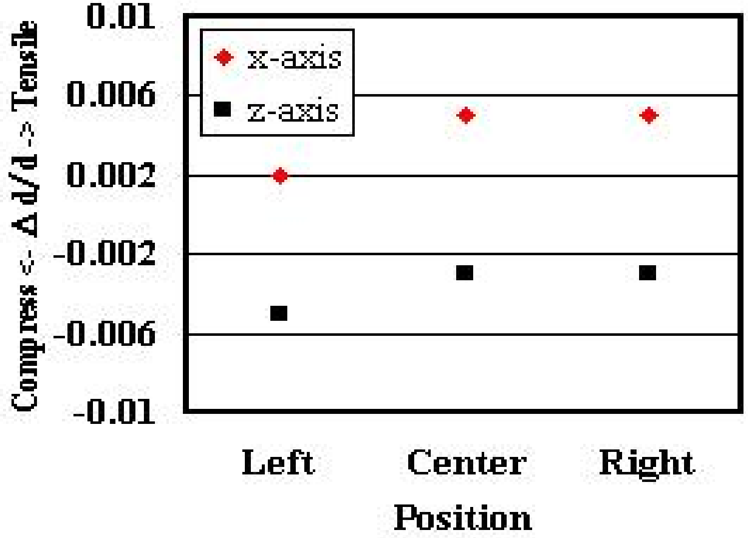




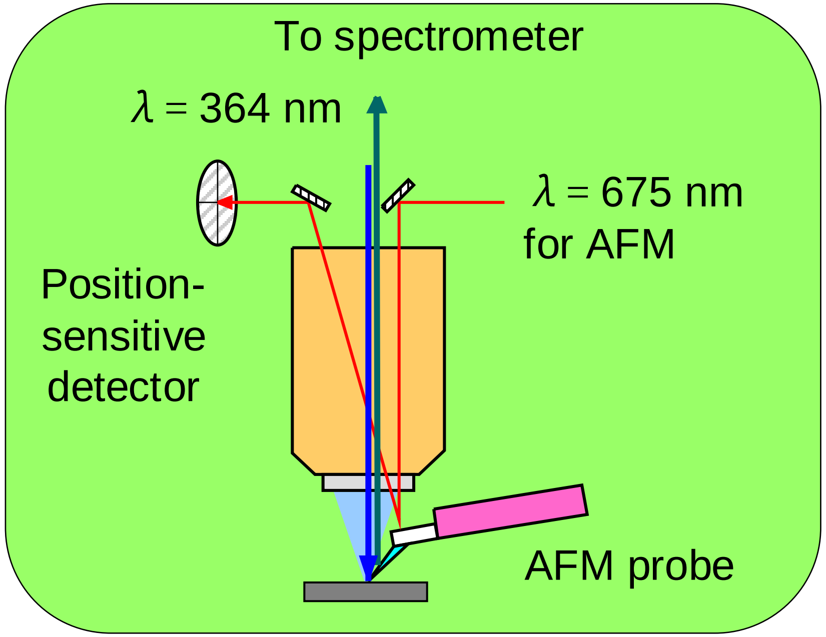
Usuda, Materials Sci. Eng. **B124–125** (2005) 143

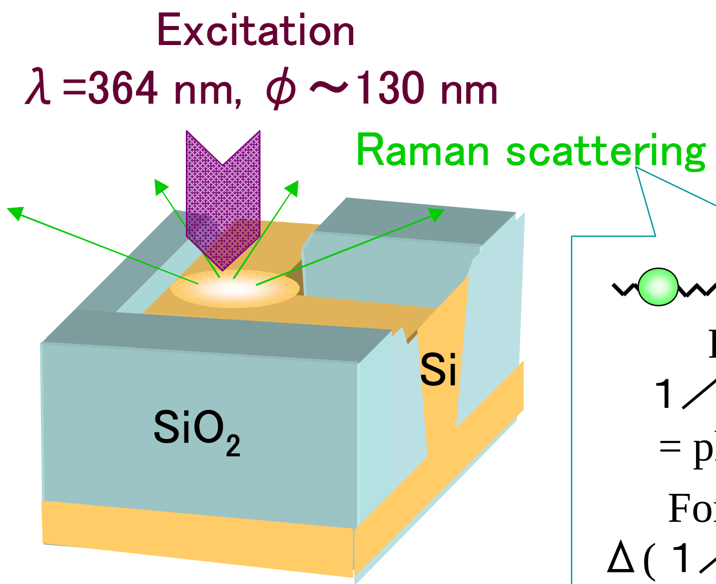


Strain in a MOSFET channel



Confocal/probe-excited UV Raman microscope for local strain analysis





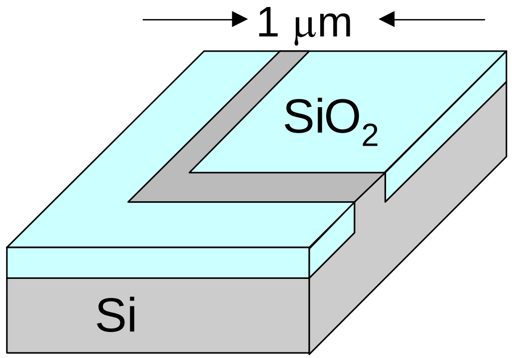
Raman shift :

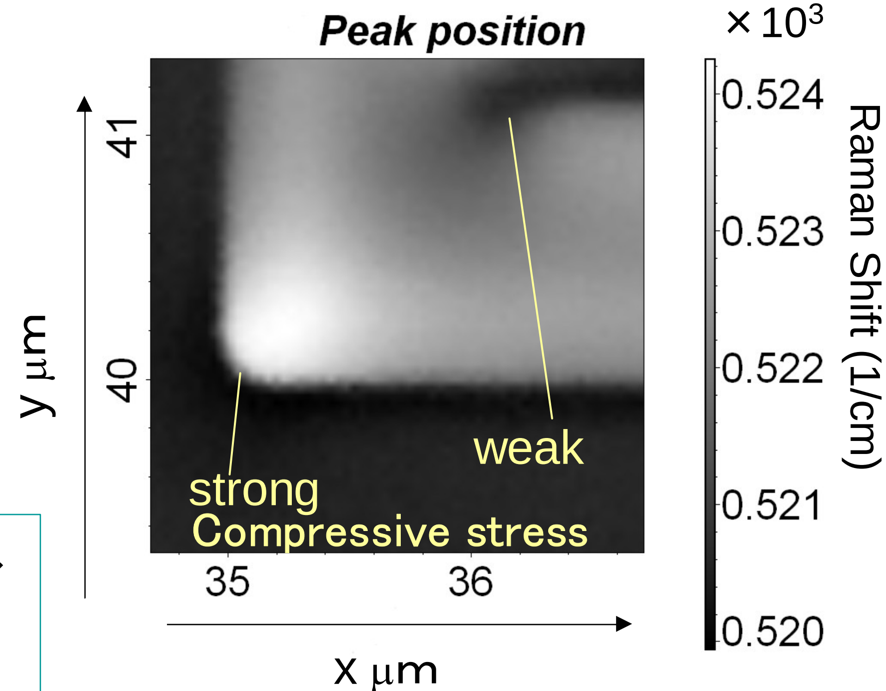
$1/\lambda_{out} - 1/\lambda_{in}$

= phonon vibration

For strain ε in Si

$\Delta(1/\lambda) = 723\ \varepsilon\ \mathrm{cm}^{-1}$

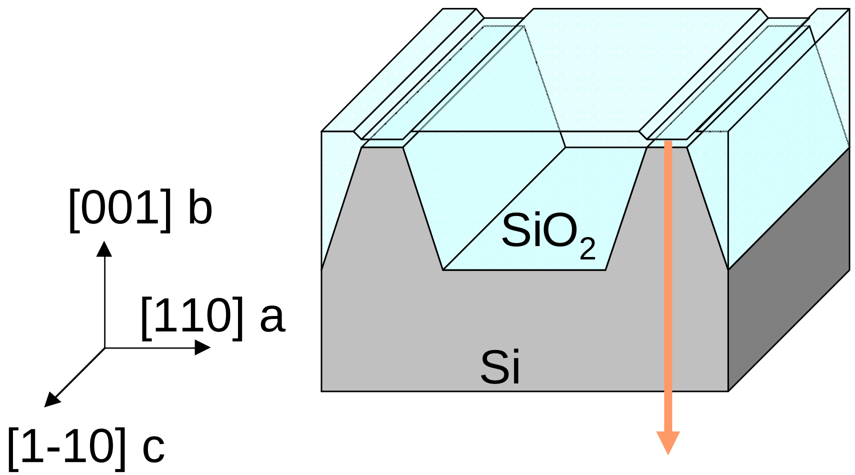


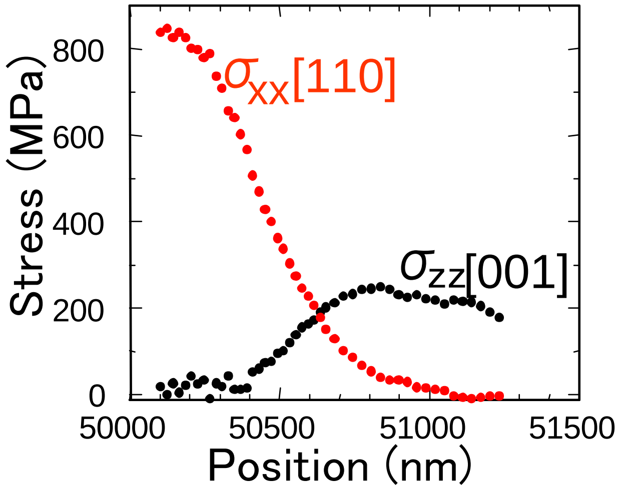


2D Raman mapping

Poborchii, Appl. Phys. Lett. **89** (2006) 233505

Raman Measurements on (110) Cross Section of STI Structure



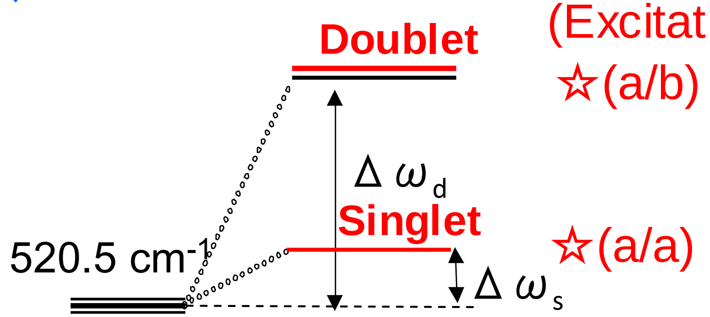


Resolving Axial Components

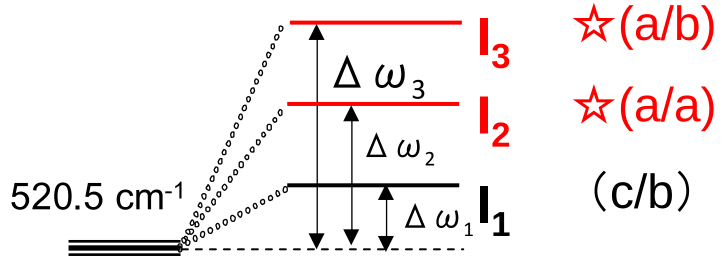
$$\Delta\omega_{ab} = C_1\sigma(100) + C_2\sigma(110)$$
$$\Delta\omega_{ab} = C_3\sigma(100) + C_4\sigma(110)$$

(110) Cross Section

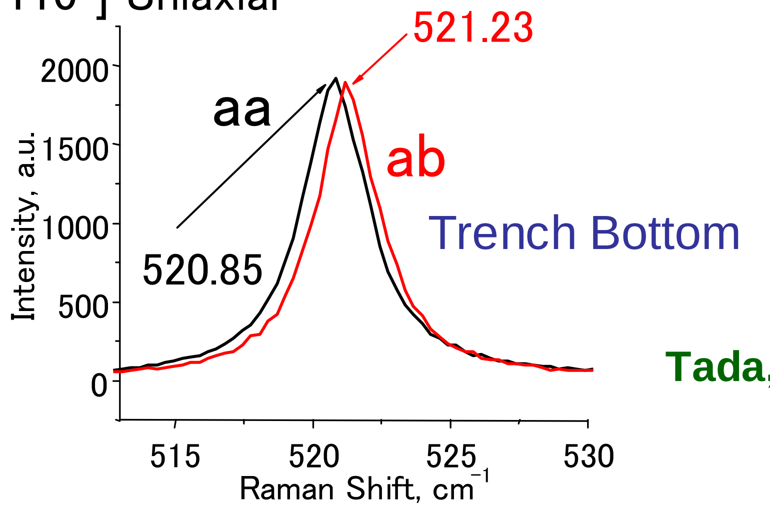
Polarization (Excitation/Detection)



[001] Uniaxial



[110] Uniaxial



Tada, SSDM 2008

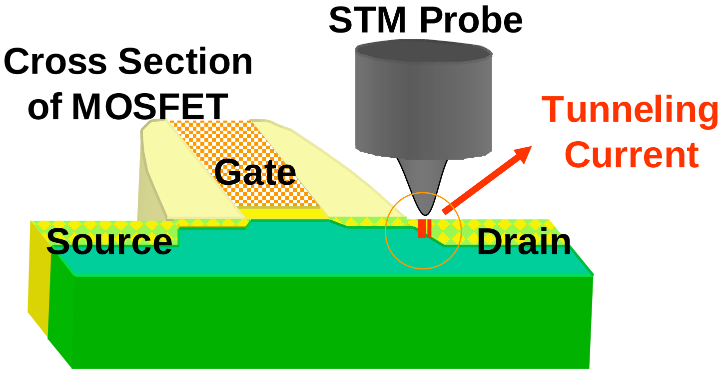
Contents

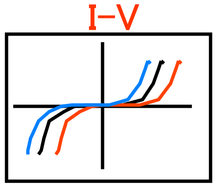
For the fabrication of Nano CMOS Transistors

What do we need?

- Gate stack (Gate dielectrics and electrode)
- Channel: Surface flatness,
  high-mobility material, Local strain
- Source/Drain: Dopant profiling for ultra-shallow junction, metal source/drain

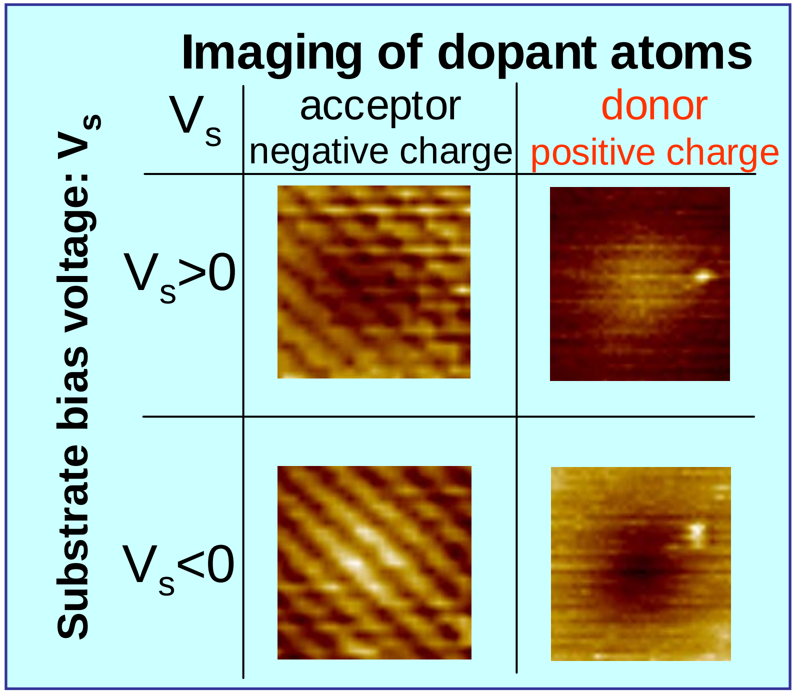
Simultaneous measurement of potential and individual dopant atoms





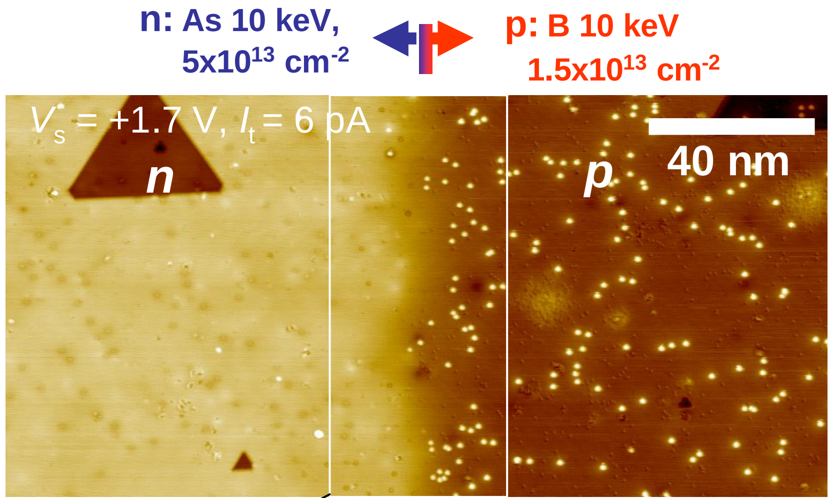
Key process

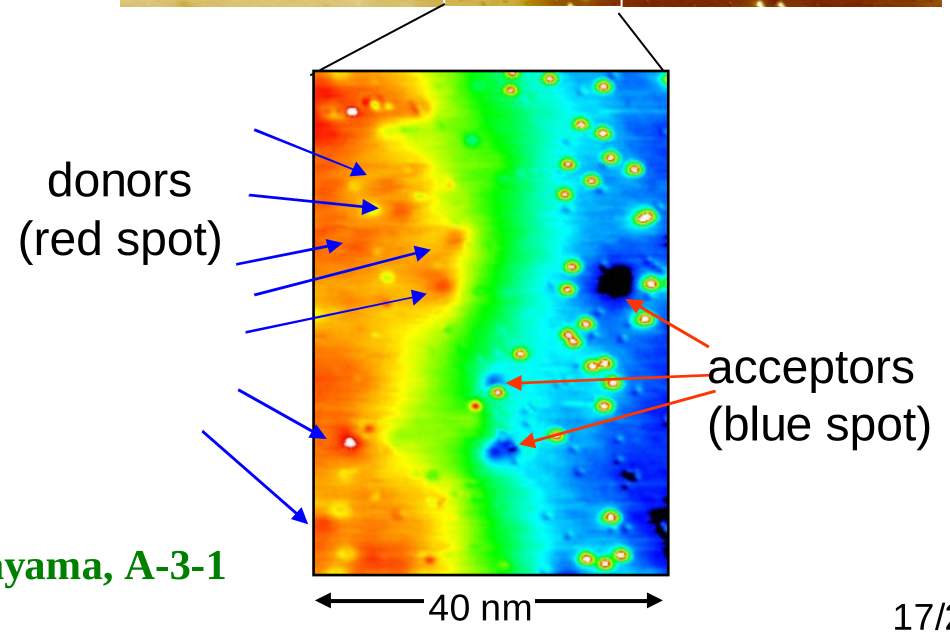
Flattening and hydrogenation of (111) surface by NH_4F treatment followed by dopant reactivation at ∼400° C



Nishizawa, Appl. Phys. Lett. **90** (2007) 122118.

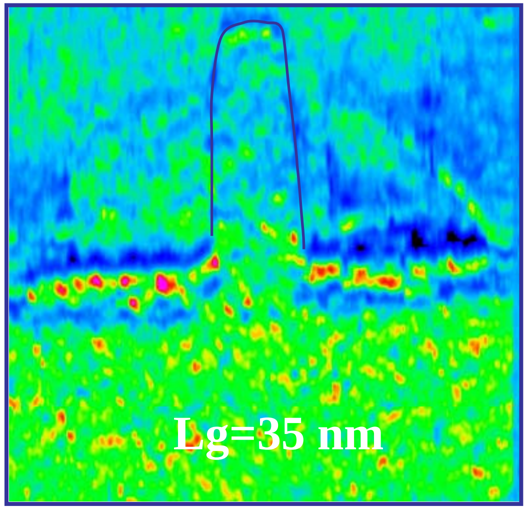
Donor distribution correlates with the potential fluctuation.

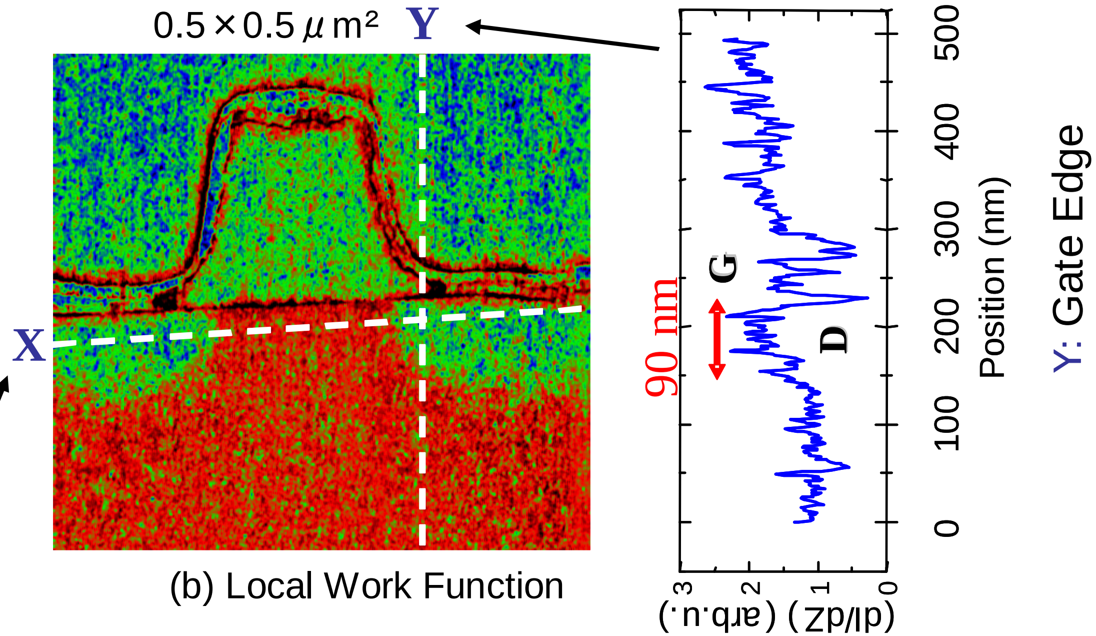


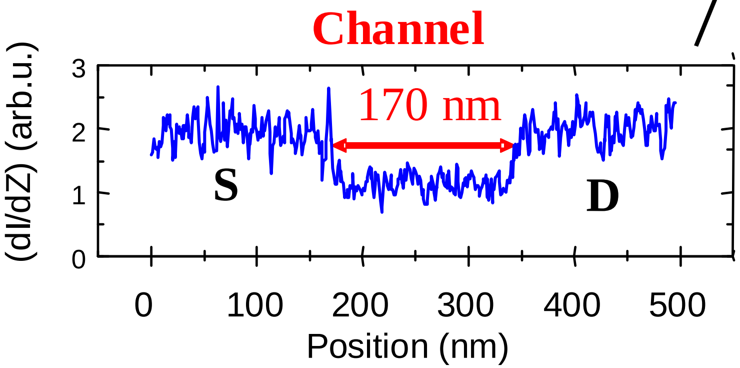


Kanayama, A-3-1

Local Work Function Measurements on a Transistor Cross Section

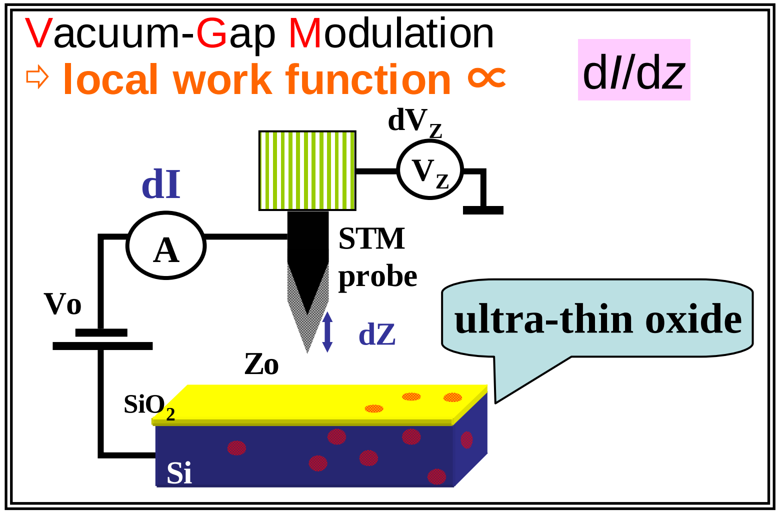






X: 30 nm below surface

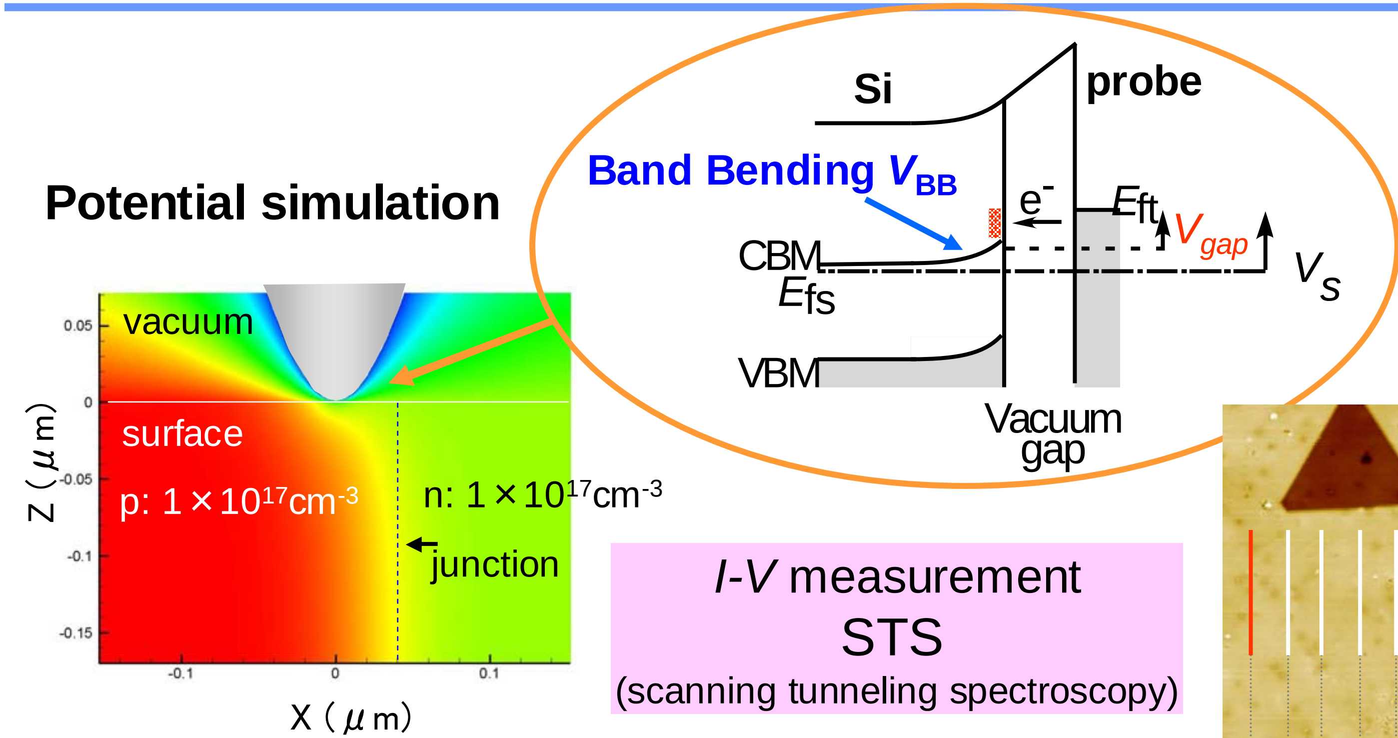
S/D: 35keV As
$2 \times 10^{15} cm^{-2}$



Bolotov, SSDM 2008

Quantitative potential profiling by *I-V* measurements

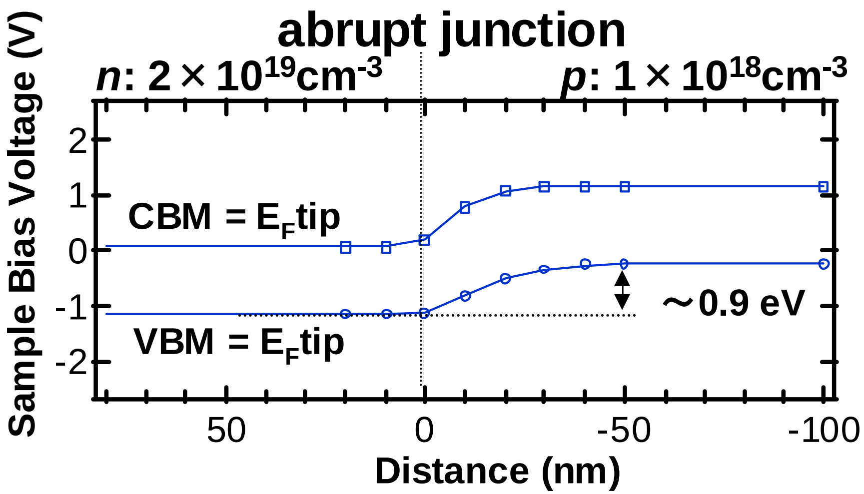
Potential simulation

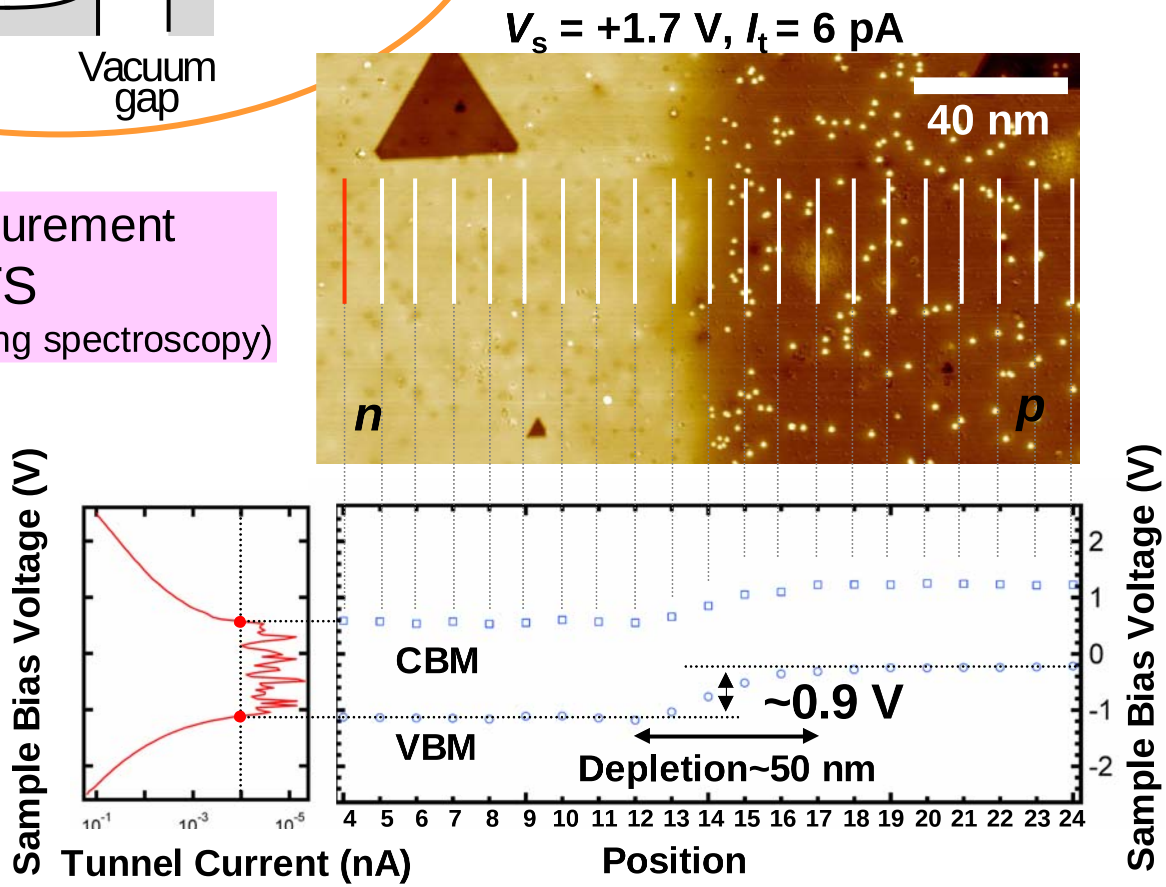


Issues

- Potential distortion by STM bias
- $V_s = V_{gap} + V_{BB}$ (V_{gap}: *unknown*)

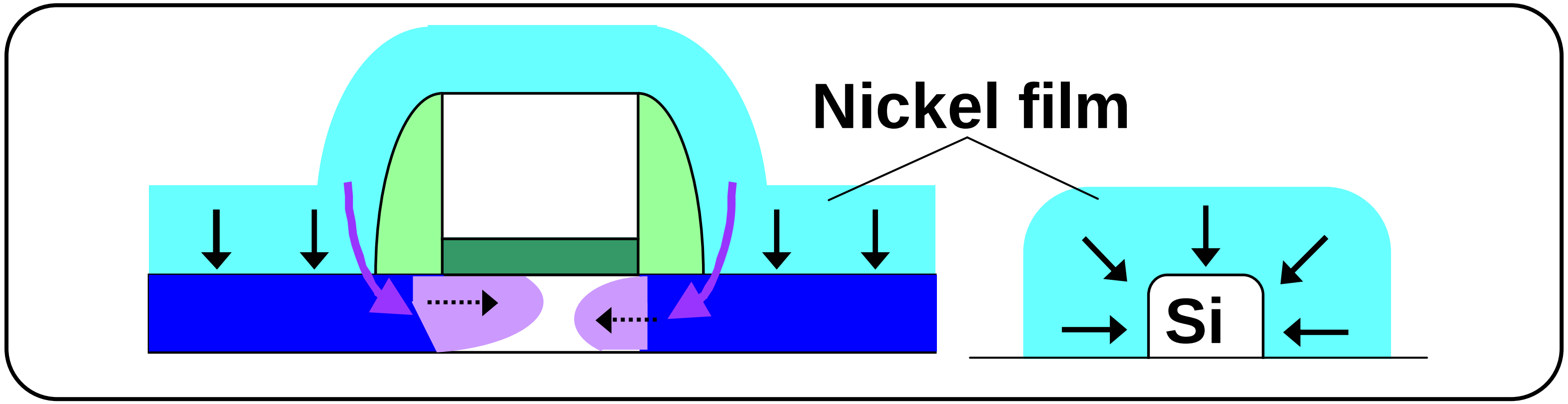
I-V measurement
STS
(scanning tunneling spectroscopy)

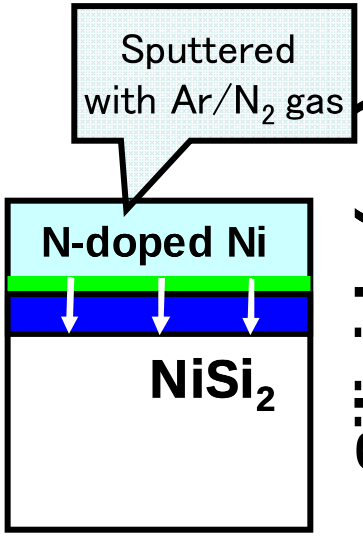




M. Nishizawa et al, APL 2007

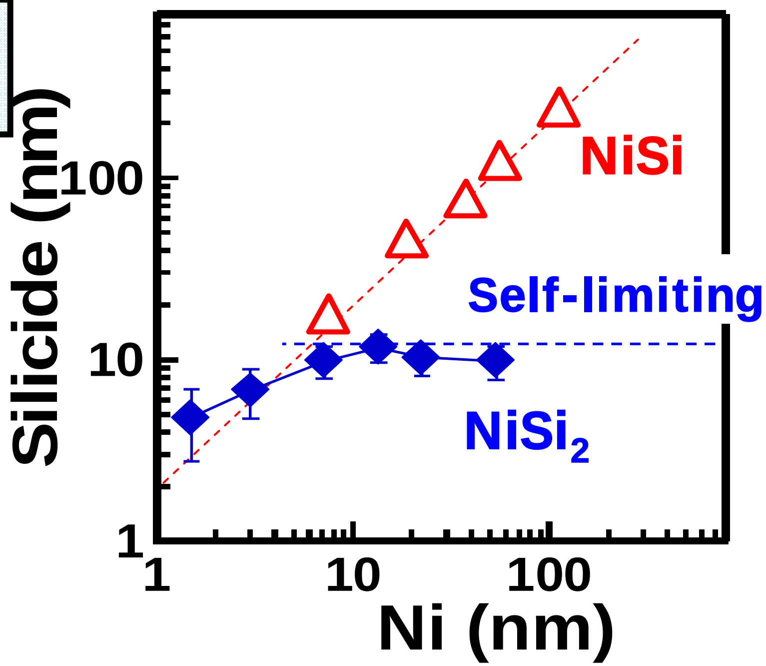
Metal S/D Formation using Epitaxial $NiSi_2$

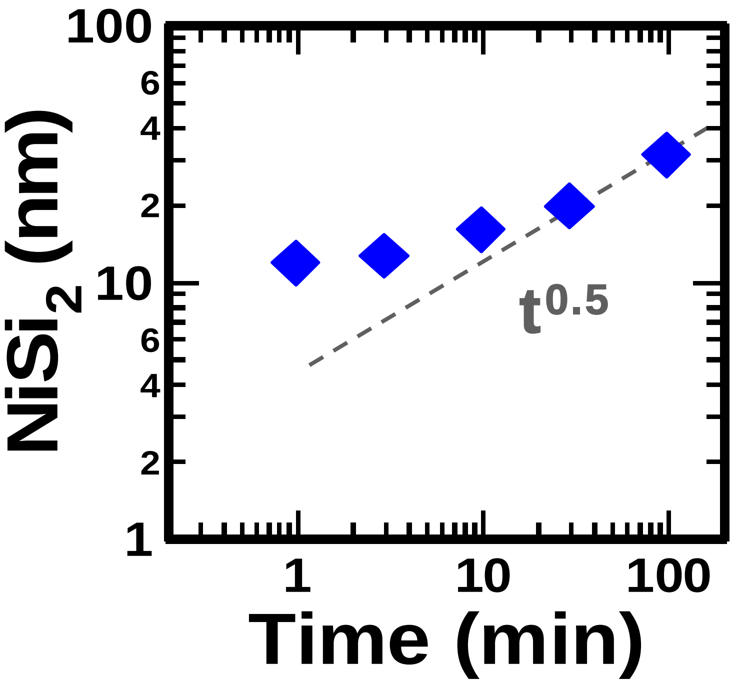




lattice diffusion

Si(100), 500ºC 1min



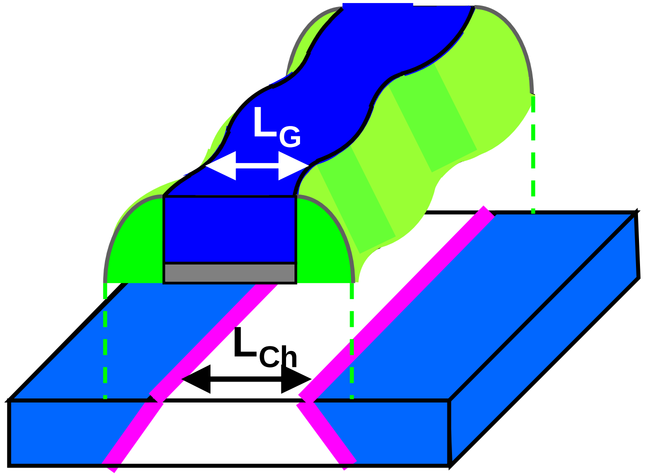


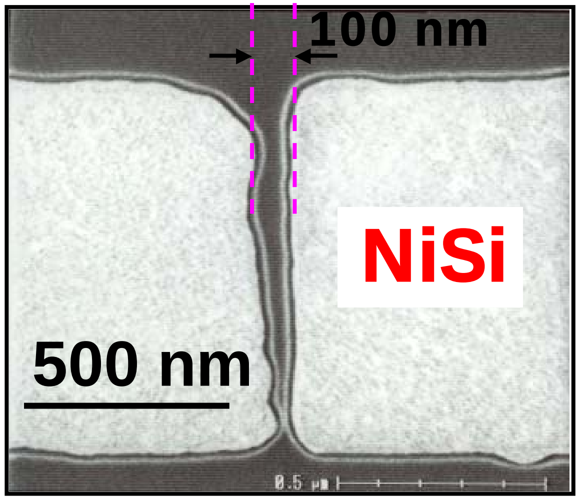
Migita, SSDM 2008

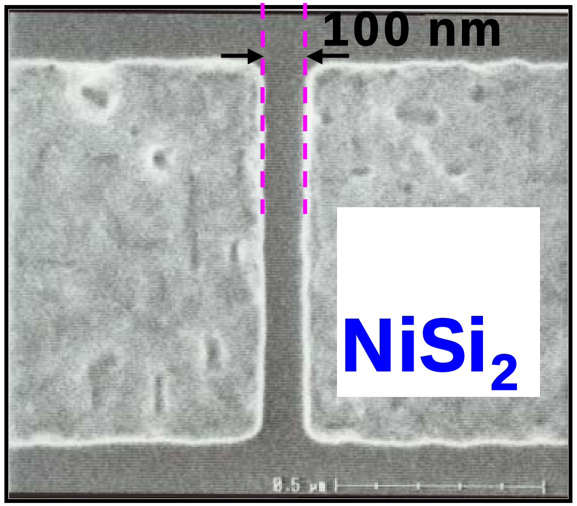
Self-limiting behavior in $NiSi_2$ growth

Metal S/D Formation using Epitaxial $NiSi_2$

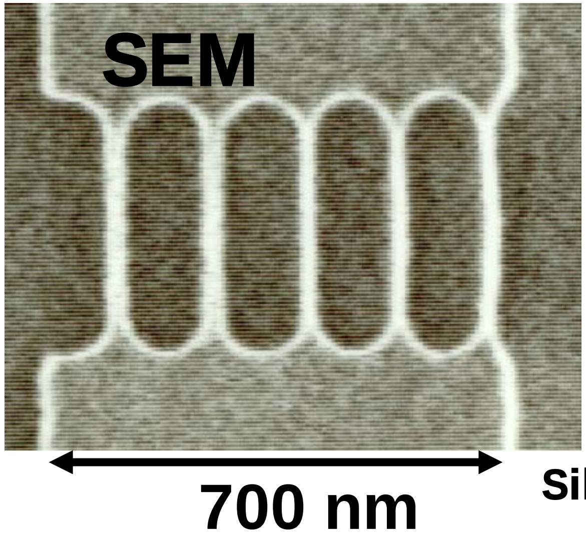
Straight edge is automatically formed.

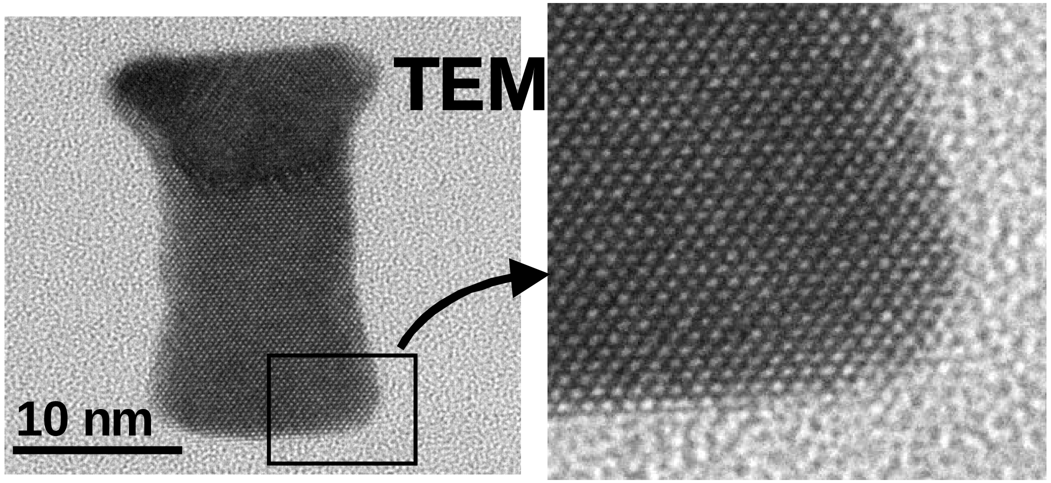






Application to Nanowire Transistor

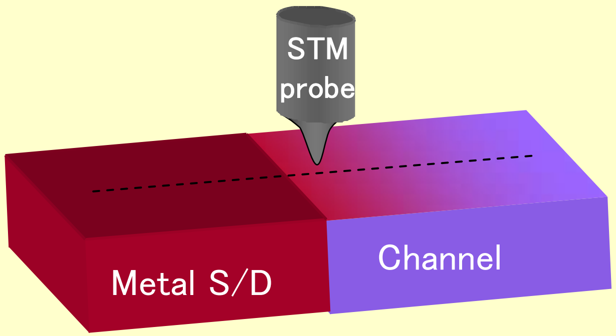


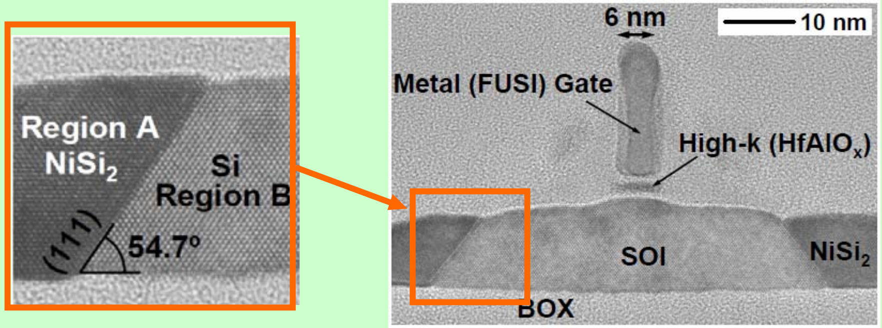


Silicidation: N-doped Ni and 500ºC anneal

towards “*Ballistic*” Transistors

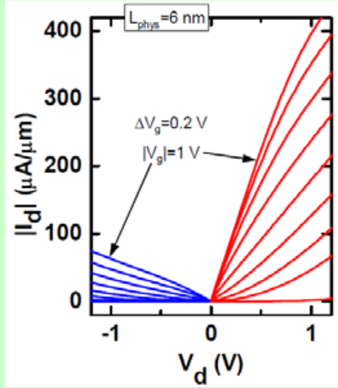
Local workfunction/barrier height measurements by STM



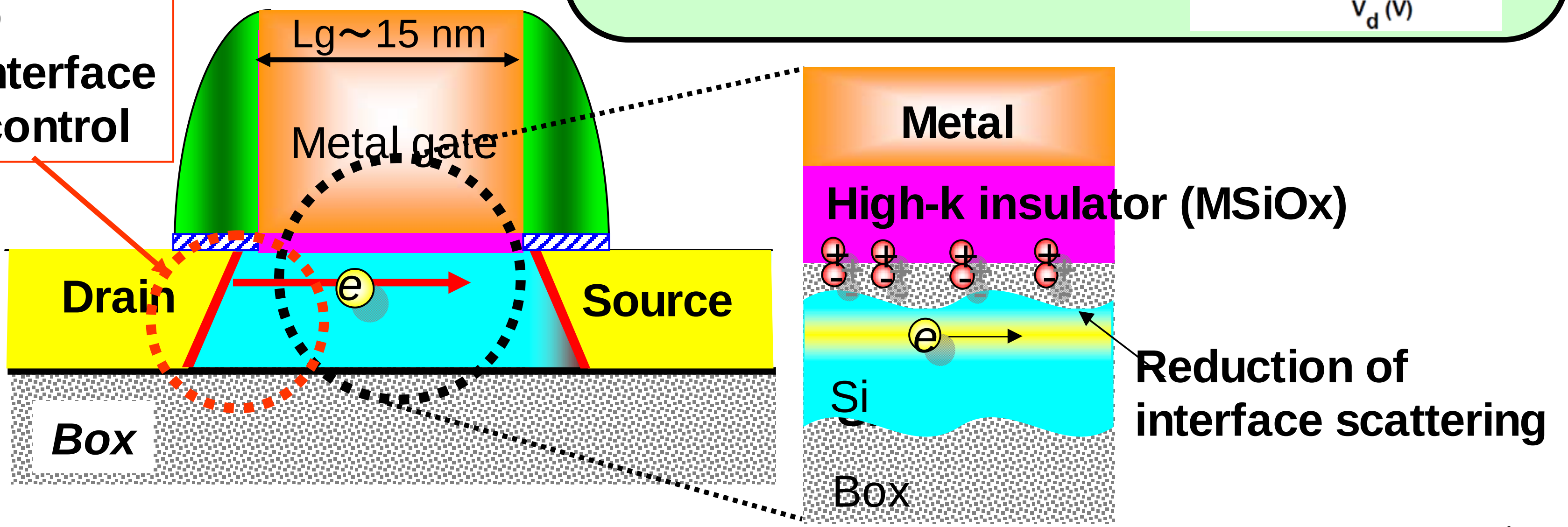


Metal S/D, High-k/Metal Gate sub-10 nm FET

- Barrier height control by dopant segregation at the $NiSi_2$/Si interface



Metal S/D
Atomically flat interface
Barrier height control



Conclusions

For Nano CMOS Fabrication;

- Atomic scale processing technologies are requires particularly at the interface of heterogeneous materials.
  - Full exploitation of Self-limiting or self-organizing phenomena
- Nanoscale characterizations of local properties and structures are needed.
  - e.g., Local strain in Si, Potential distributions

Acknowledgments

Colleagues in MIRAI project

T. Tada and V.V. Porochii for UV Raman measurements

L. Bolotov and M. Nishizawa for STM measurements

K. Usuda for Nano-beam diffraction

N. Hirashita, T. Numata, T. Tezuka, N. Sugiyama and S. Takagi and many other members of the MIRAI project for providing STI and strained SOI structures

Sample preparation

N. Hattori of Renesas Technology for strained STI structures

H. Fukutome of Fujitsu Laboratory Ltd. for the *p-n* junction samples.

This work was supported by MIRAI project, NEDO and by METI under the Innovation Research Project on Nanoelectronics Materials and Structures.