Abstract of Presentation

Presentation Title:

Atomic level material processing and characterization for nanoscale CMOS transistors

(Toshihiko Kanayama)

Abstract :

The continued miniaturization of Si CMOS devices is now facing various fundamental difficulties. It will no more be straightforward to enjoy the long-lasting scaling merit that the transistor drive current is yearly increased while keeping the leakage current small enough. To circumvent this situation, several technology boosters such as strain-enhanced channel mobility, high-k gate dielectrics/ metal gate electrode and metal source/drain are being introduced into the CMOS technology in conjunction with the new transistor structures to suppress the short channel effects, e.g., multi-gate and nano-wire structures.

The implementation of these new materials together with the structural complexities obviously requires atomic scale processing technology particularly at the interface of heterogeneous materials. Moreover, as the physical dimension shrinks, device performance is getting more vulnerable to small fluctuations in structures, which is becoming a limiting factor of miniaturization.

To meet these requirements, we are working on atomic control techniques of several interfaces. An example is flattening of Si surfaces and subsequent high-k film deposition to improve the leakage current and the channel mobility. The tight control is also needed at the metal/Si interface. A possible solution to this problem is the use of epitaxial $NiSi_2$ silicide, which yields abrupt interfaces even in nano-wire structures. The energy barrier at the metal/Si interface may be controlled by placing suitable impurities at the interface.

The development of these new processes involves tremendous challenges in metrology and characterization techniques. The solutions may be found in such nanotechnology tools as scanning probe microscopes. As an example, atomic level profiling is presented in dopant and carrier concentrations using the scanning tunneling microscopy.

This work was supported by NEDO, Japan as part of the MIRAI project and by METI under the Innovation Research Project on Nanoelectronics Materials and Structures.