Development of quantum hardware towards fault-tolerant quantum computing

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Fault-tolerant quantum computer = “Perpetual” quantum machines
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Many world !!!!

\( O(2^N) \)
Fault-tolerant quantum computer = “Perpetual” quantum machines
Quantum supremacy using a programmable superconducting processor

- Flip-chip bonding
- Frequency-tunable qubits
- Tunable-coupler architecture
  - Fast two-qubit gate ~ 12 ns
  - Small residual coupling

Google AI Quantum
Nature 574, 505 (2019)

<table>
<thead>
<tr>
<th></th>
<th>Average error</th>
<th>Isolated</th>
<th>Simultaneous</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-qubit ($e_1$)</td>
<td>0.15%</td>
<td>0.16%</td>
<td></td>
</tr>
<tr>
<td>Two-qubit ($e_2$)</td>
<td>0.36%</td>
<td>0.62%</td>
<td></td>
</tr>
<tr>
<td>Two-qubit, cycle ($e_{20}$)</td>
<td>0.65%</td>
<td>0.93%</td>
<td></td>
</tr>
<tr>
<td>Readout ($e_r$)</td>
<td>3.1%</td>
<td>3.8%</td>
<td></td>
</tr>
</tbody>
</table>

9 × 6 – 1 = 53 qubits
Fixed-frequency qubits

- Long coherence ~ 100 μs
- Cross-resonance gate ~ 150 ns
- 16-bit GHZ state generation
- 20-bit, 53-bit cloud service

K.X. Wei et al. arXiv:1905.05720 (IBM)

### Table: IBM Q System One
(In preparation for the IBM Q Network)

<table>
<thead>
<tr>
<th></th>
<th>IBM Q System One</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relaxation (T1) in μs</td>
<td>73.9</td>
</tr>
<tr>
<td>mean</td>
<td>132.9</td>
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<tr>
<td>best</td>
<td>38.2</td>
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<tr>
<td>worst</td>
<td></td>
</tr>
<tr>
<td>Dephasing (T2) in μs</td>
<td>69.1</td>
</tr>
<tr>
<td>mean</td>
<td>100.8</td>
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<tr>
<td>best</td>
<td>39.2</td>
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<tr>
<td>worst</td>
<td></td>
</tr>
<tr>
<td>Two-qubit (CNOT) error</td>
<td>1.69</td>
</tr>
<tr>
<td>mean</td>
<td>0.97</td>
</tr>
<tr>
<td>best</td>
<td>2.85</td>
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<tr>
<td>worst</td>
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</tr>
<tr>
<td>Single-qubit error</td>
<td>0.41</td>
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<tr>
<td>mean</td>
<td>0.19</td>
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<tr>
<td>best</td>
<td>0.82</td>
</tr>
<tr>
<td>worst</td>
<td></td>
</tr>
</tbody>
</table>

53 Qubit Rochester Device

https://www.ibm.com/blogs/research/2019/03/power-quantum-device/
Parametric coupling

- Fixed- and tunable-freq qubits
- 16-bit cloud service

Resonator mediated coupling

- Tunable qubits
- 49-bit chip under development

Quantum bus coupling

1 resonator + 20 frequency tunable qubits
All-to-all coupling
18bit GHZ state generation

C. Song et al. Science 365, 574 (2019) (Zhejiang)
2D integration with vertical access

- Spring array
- Flip-chip cover
- Integrated qubit chip
- Contact probes
- Coaxial cables
- Superconducting through silicon vias
- Al package
- Superconducting bump contact
- Coaxial cables
“Smart” brute force

Improved coherence materials fabrication

Fast gate/ readout design architecture

Better packaging/ wiring filtering, shielding, thermalization high-density, miniaturized components

Peripheral technologies control electronics SFQ/ CryoCMOS cryogenics

low-latency, all-digital?
New directions beyond brute force

Robust qubits (0-π qubit, etc.)

Bosonic codes (cat, binomial, GKP, etc.)

Temporal-mode entanglement
+ Measurement-based quantum computing

Distributed quantum computing


arXiv:1907.12487 (Yale)

Nature 558, 264 (2018) ETH Zurich
Current state-of-the-art of ion trap quantum computing

High-fidelity operations achieved in few-qubit systems

- Single-qubit gate: 99.9999 %
- Two-qubit gate: 99.9 %
- SPAM: >99.9%

Advantages of using trapped ions:
- Long coherence times (~ 1 min)
- Identical qubits (cf. atomic clocks)
- Room temperature operation
- All-to-all qubit connection

Disadvantages:
- Slow gate speed
- Difficult to scale beyond >50 qubits

PRL 113 220501(2014); PRL 117 060504(2016) Oxford

IonQ quantum computer:
- Fully connected 11 ions
- >60 2-qubit gates w/ error < 1.0%
- Partnered w/ Microsoft Quantum Azure

Other leading institutions:
- NIST
- U. Innsbruck
- PTB
- U. Oxford
- U. Maryland
- ETH Zurich
- Honeywell
- Alpine Quantum Technologies
Prospects for ion trap quantum computing

Increasing numbers of ions in a 1D chain increases difficulties of quantum operations due to motional mode crowding. **Multi-trap architecture needed for >100 qubits.**

**Quantum CCD**

- Separate trapping and interaction zones
- Ion shuttling on 2D electrode structure
- Microwave gate integration
- NIST, PTB, U.Sussex

**Optical interconnect**

- Trap modules connected via photons
- High modularity

*Photo by TIQI group, University of Maryland*
Recent trends in photonic quantum computing

**Boson sampling**
- 20 photons in 60 modes
- arXiv:1910.09930
  (Univ. of Science and Technology of China)

**NISQ algorithms**
- Variational quantum eigensolver
- Quantum Hamiltonian learning
  - Nat. Commun. 5, 4213 (2014)
  (Univ. of Bristol)

**Integrated photonic chips**
- >550 components on a single chip
  (Univ. of Bristol)

**Large-scale continuous-variable cluster states**
- 5x5000
  - 2D cluster states
  - Science 366, 373 (2019)
    (Univ. of Tokyo)
  - Science 366, 369 (2019)
    (Technical Univ. of Denmark)
Future prospects for large-scale fault-tolerant photonic QC

Architecture for scalable & universal quantum computing

Time-domain multiplexed one-way quantum computation

High quality photonic circuits based on photonic chips & fibers

Free-space optical circuits

Photonic chip

Fiber delay line

Bosonic codes for fault-tolerant quantum computation

One optical pulse represents one logical qubit (cat/binomial/GKP code) => efficient!

Example: GKP code + continuous-variable quantum gates

⇒ Realistic threshold for fault-tolerant quantum computation (~10dB of squeezing)
High-fidelity control and readout in scalable architecture
Quantum error correction
Fault-tolerant quantum computing

NISQ (noisy intermediate scale quantum technology)
Fault-tolerant universal quantum computer

https://www.jst.go.jp/moonshot/sympo/sympo2019/wg6_e.html
Quantum computing research will inevitably (and hopefully) be as disruptive, controversial, provocative, and philosophical as we have seen in the history of quantum mechanics.