JPMJMS2065

Large-Scale Silicon Quantum Computer

7/20/2023

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Principal Investigators (PIs)

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Kobe Univ.
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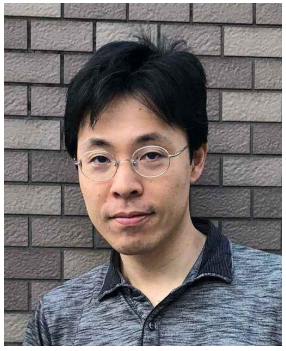


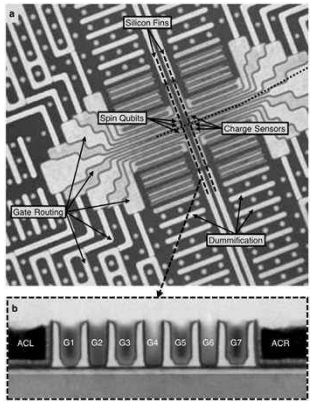
RIKEN
T. Nakajima

Tokyo Tech
J. Yoneda

Background and motivations

- Scaling is one of the advantages of silicon qubits, but in fact they have only achieved up to 6 qubits.
- In other words, large-scale integration is still a challenge.

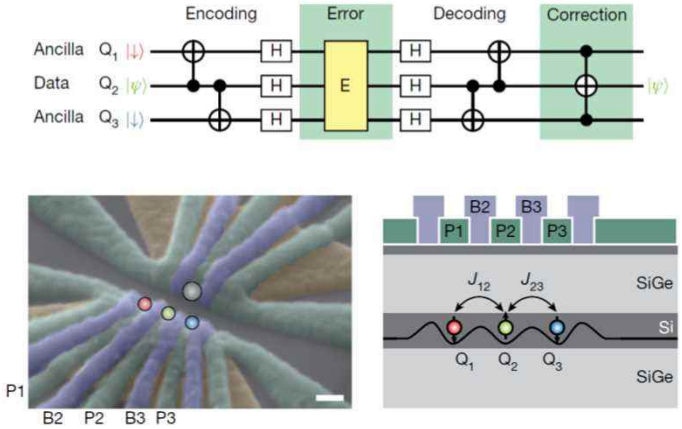
nMOS Intel + QuTech (2021)



arXiv:2101.12650

28Si w/
300mm wafer

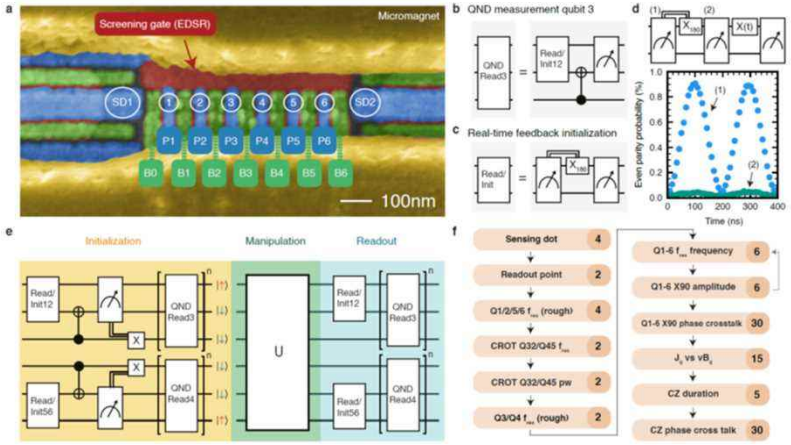
SiGe RIKEN (2022)



https://www.nature.com/articles/s41586-022-04986-6

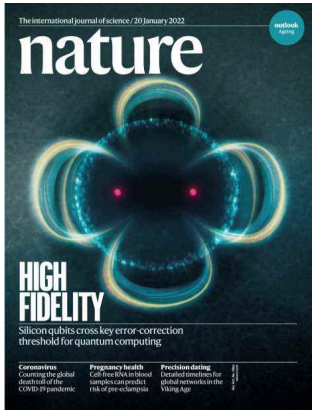
3 qubits & Quantum error correction

QuTech + TU Delft (2022)



https://arxiv.org/abs/2202.09252

6 qubits



Special issue of Nature on silicon quantum computers

1/20/2022

https://media.nature.com/original/magazine-assets/d41586-022-00047-0/d41586-022-00047-0.pdf

Silicon qubits get closer to achieving error correction

Ada Warren & Sophia E. Economou

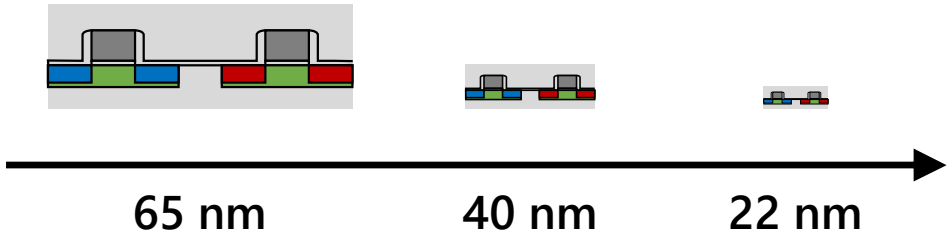
The results of all three groups move silicon-based quantum-information processing a step closer to offering a viable quantum-computing platform.

The next experimental milestone for this system would therefore be to build a larger array of quantum dots hosting two-qubit gates with fidelities as high as those demonstrated by Xue et al. and Noiri et al., despite the presence of more qubits. A further breakthrough for such a system would be the demonstration of quantum error correction.

Expectations for silicon semiconductor technology

- The question is whether the current silicon qubits are taking full advantage of silicon semiconductor technology.
- Silicon semiconductor technology has two major aspects.

(1) Miniaturization of devices



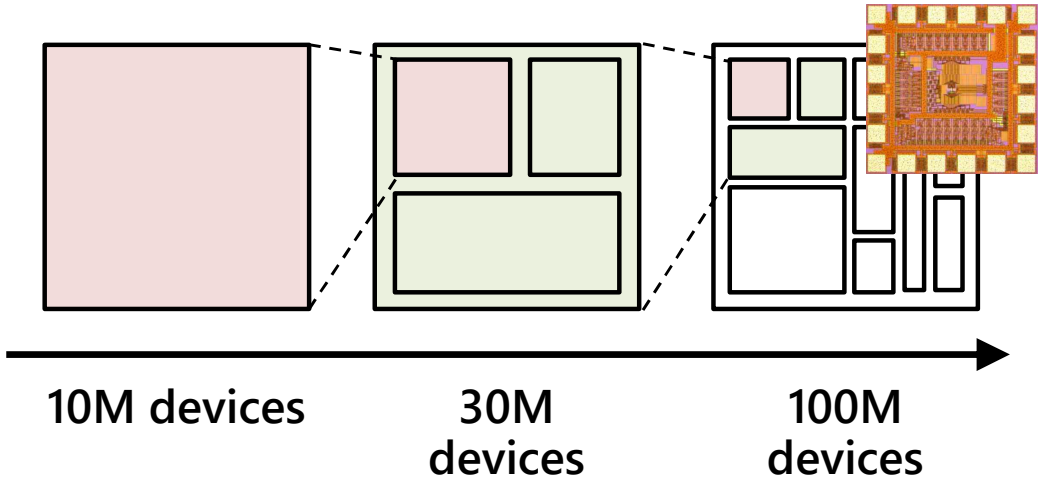
Pros

- ✓ Optimize qubit structure (Size, distance, etc.)

Cons

- ✓ Increase noise (crosstalk etc.)

(2) Integration of a large number of devices



Pros

- ✓ Obtain a large number of qubits with remarkable uniformity
- ✓ Handle a large number of wires from qubit arrays by embedding CMOS circuitry
- ✓ Achieve high-precision control of qubit arrays

Cons

- ✓ Result in high heat density

We need to take advantage of both of these two aspects.

Our approach (Top-Down Approach)

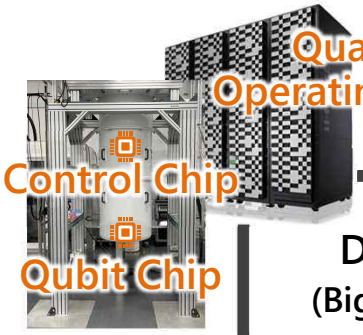
■ Approach changed to take full advantage of silicon semiconductor technology

OUR PROJECT

Top-Down Approach

Firstly, we integrate a large number of qubits and then improve the "quality" of these qubits with various technologies.

Quantity (# of Qubits)



GOAL

Digital Technologies
(Big data, Digital twin etc)

Semiconductor Technologies
(Integrated circuits)

START

CONVENTIOANL

Bottom-Up Approach

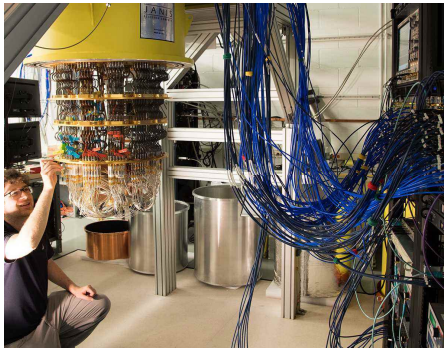
Increase # of qubits 1, 2, 3, ...

Focusing on "quality" and starting with a single qubit and increasing the number step by step.

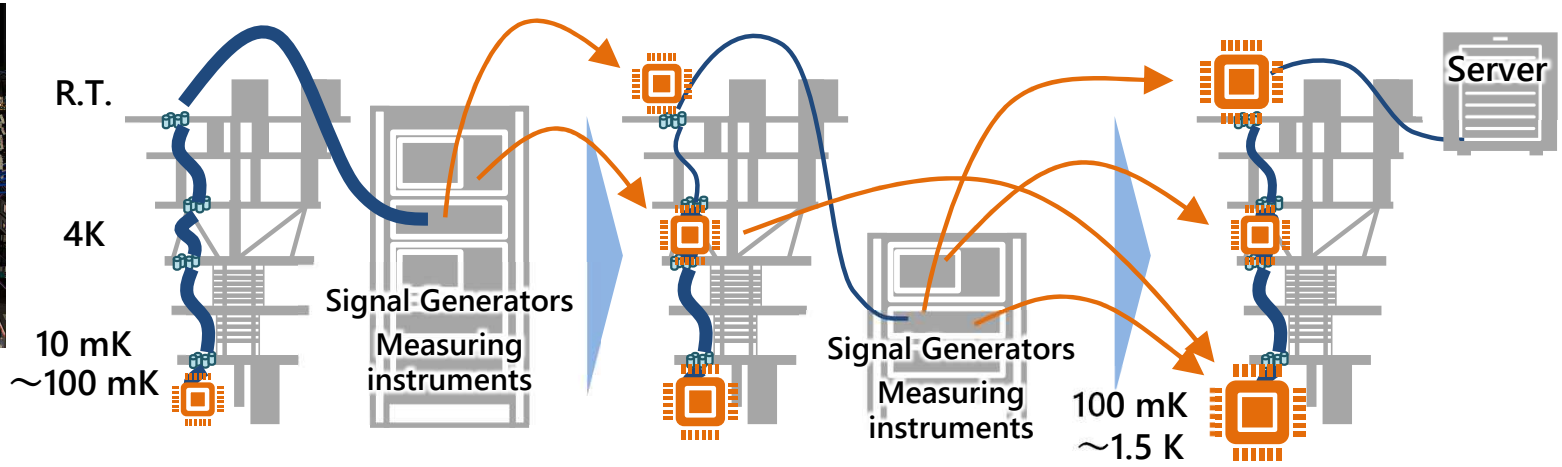
Quality (Fidelity)

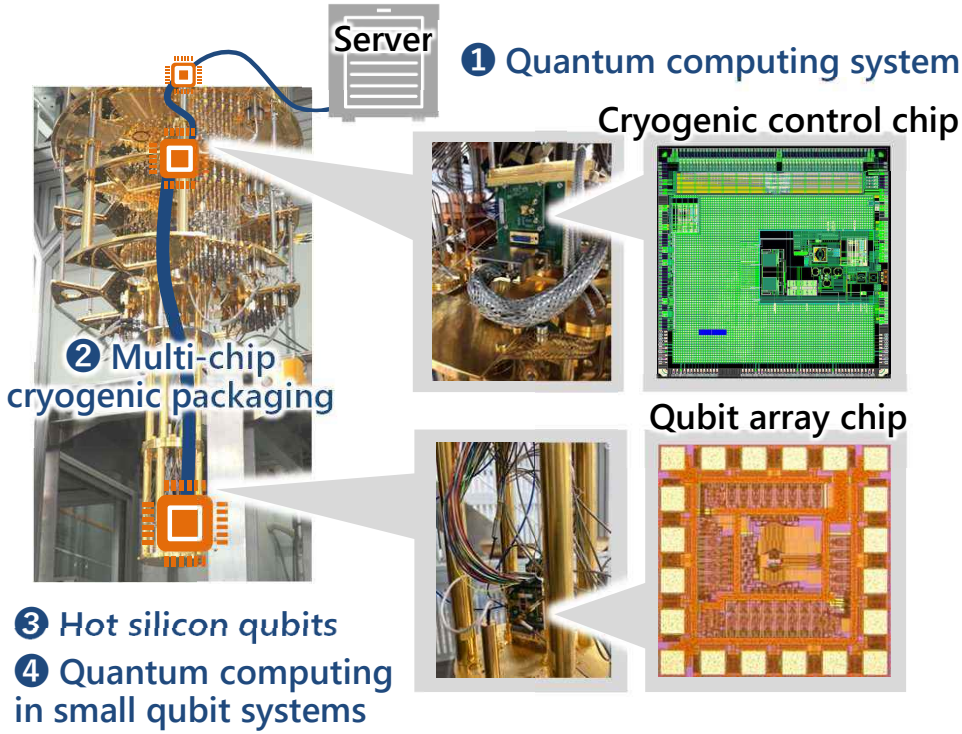
Large-scale silicon quantum computer

■ The final goal is to implement almost all elements in a single fridge.



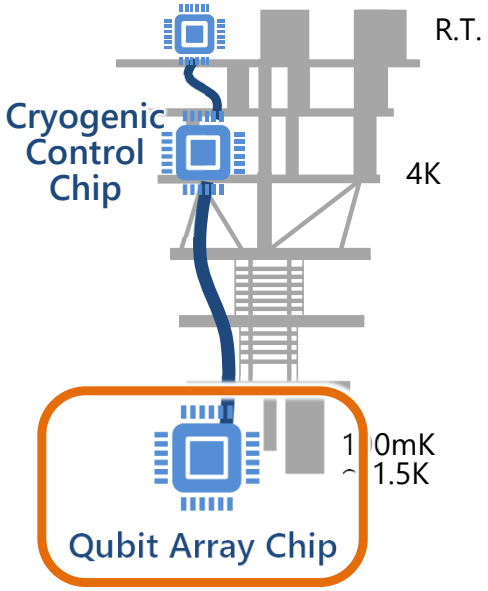
https://spectrum.ieee.org/tech-talk/semiconductors/design/google-team-builds-circuit-to-solve-one-of-quantum-computings-biggest-problems

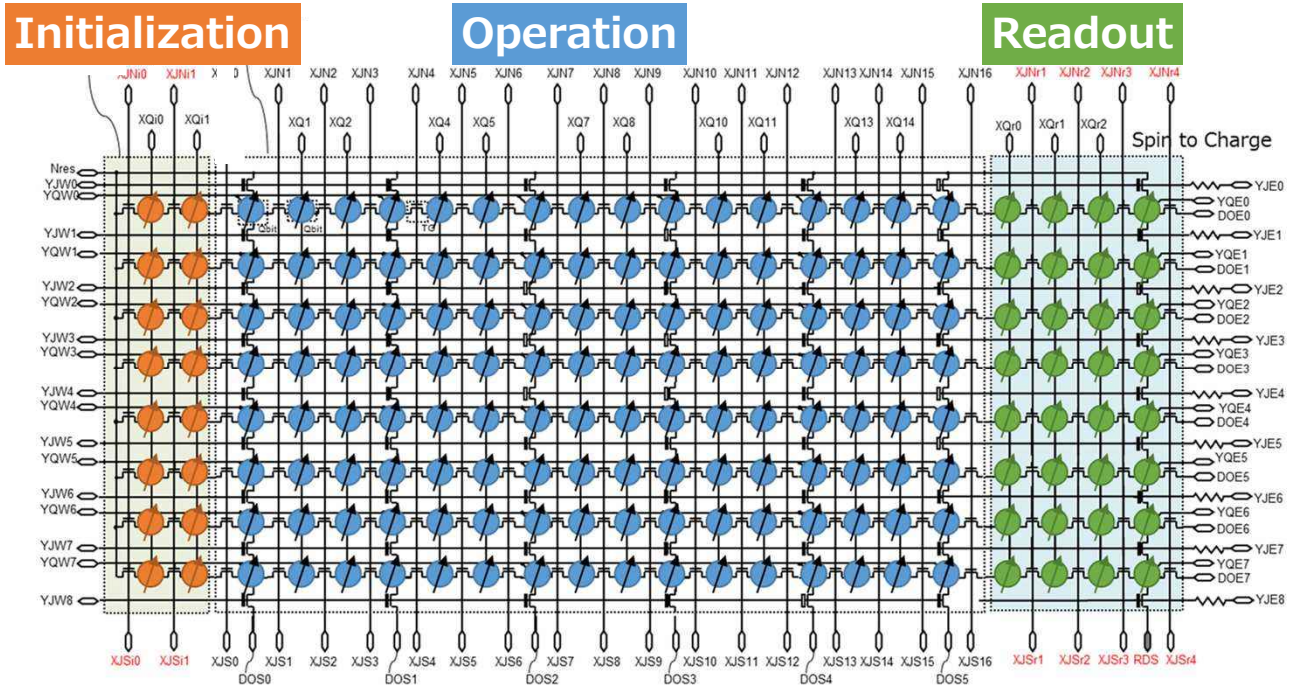




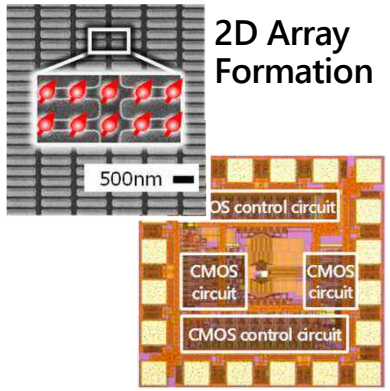
R&D Themes	PIs
❶ Quantum computing system	Hitachi/ Hiroyuki Mizuno
❷ Multi-chip cryogenic packaging	Kobe Univ./ Makoto Nagata
❸ Hot silicon qubits	Tokyo Tech/ Tetsuo Kodera
❹ Quantum computing in small qubit systems	Tokyo Tech/ Jun Yoneda RIKEN/ Takashi Nakajima

Qubit array chip



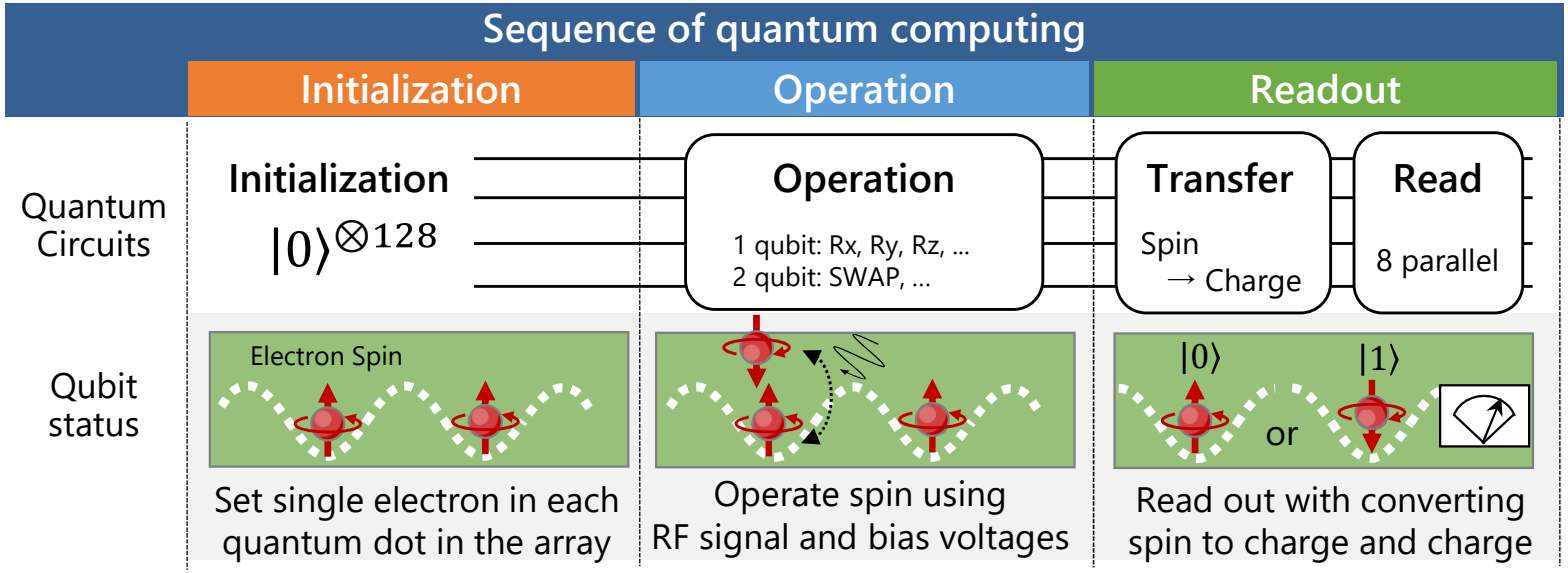


Formation of Quantum dots array



Integrate CMOS circuits on the same die

Sequence of quantum computing



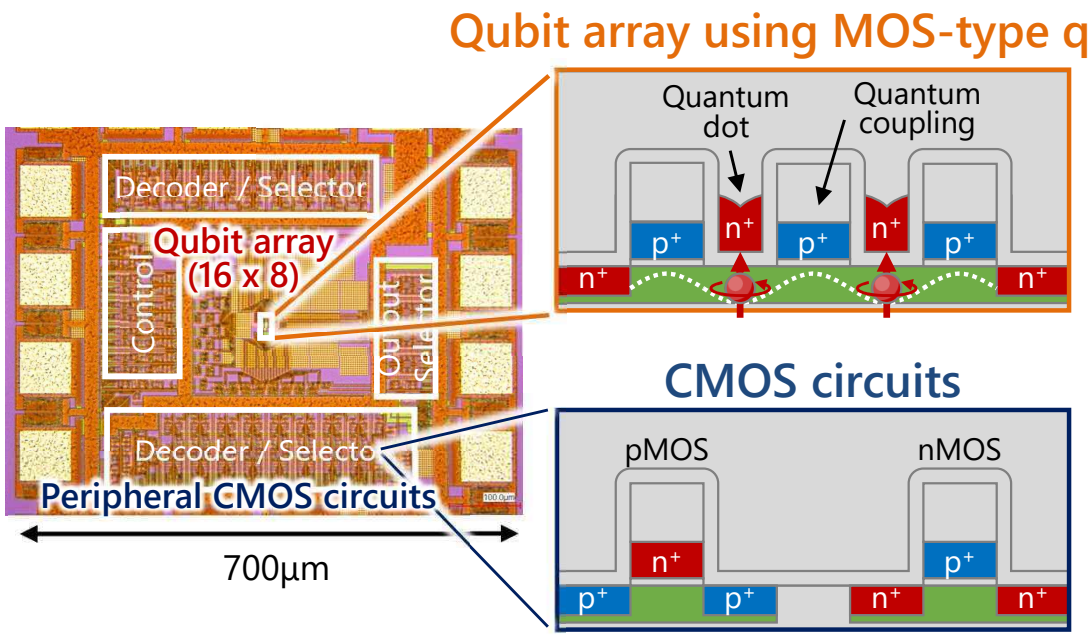
Set single electron in each quantum dot in the array

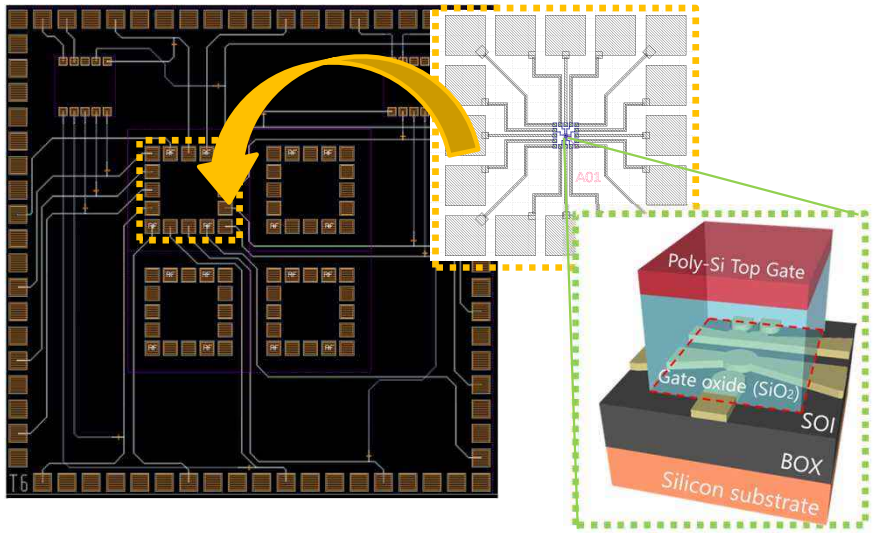
Operate spin using RF signal and bias voltages

Read out with converting spin to charge and charge to current

Formation of quantum dots array and integration of CMOS

- Developed a “Embedded-Qubit CMOS process (QCMOS),” which integrates qubit arrays and the peripheral circuits that control it on a single die.
- Developed a “Active Si interposer" that can integrate circuits on an interposer.





✓ On-chip CMOS control circuitry can manage a large number of wires from a qubit array.

65-nm Embedded-Qubit CMOS process (QCMOS)

✓ Heterogeneous integration is possible. (SiGe + CMOS)

180-nm Active Si interposer

Lee N. et al. 2021 Int. Conf. on SSDM A-1–02 (2021)
N. Lee et al., Jpn. J. Appl. Phys. 61, SC1040 (2022)

Initialization of qubit array

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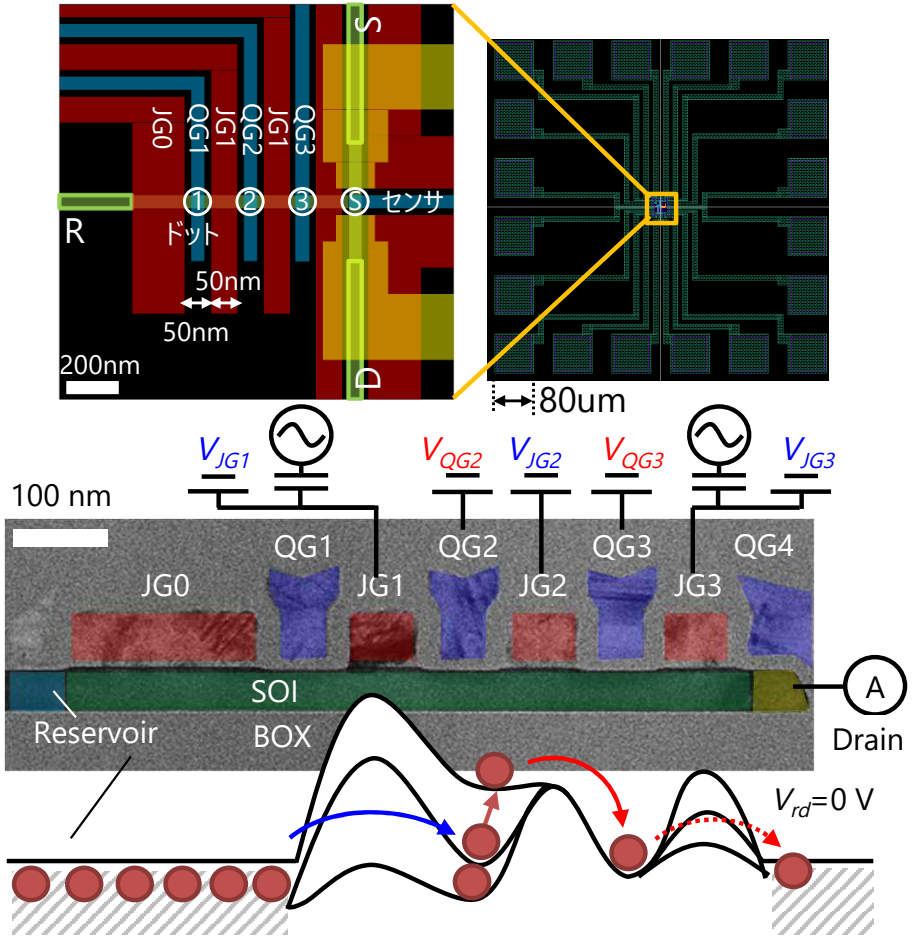
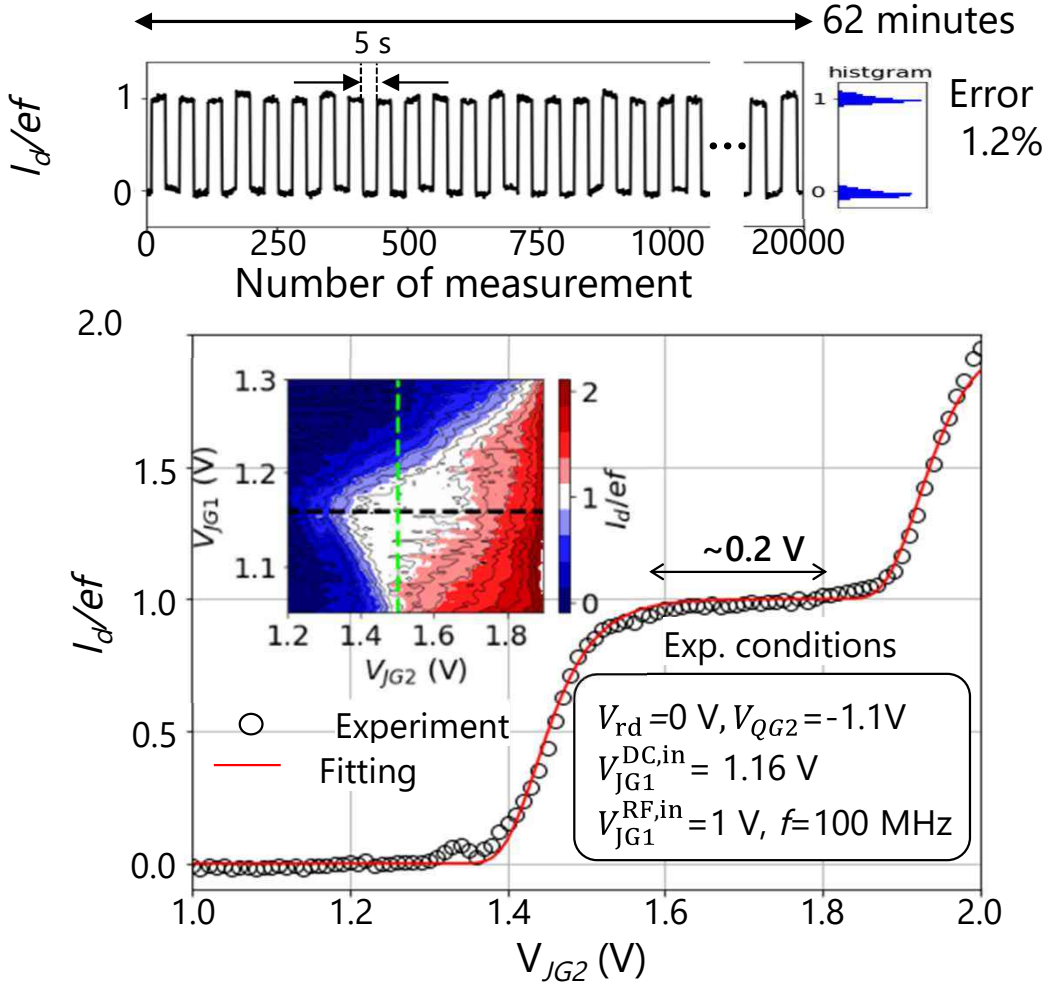
- Developed single-electron pumping technique for highly reliable initialization.
- Demonstrated 100 MHz single-electron pump transport with 1 hour stability and 99% accuracy at 4K.



Small-scale experimental circuits



Single-electron pumping

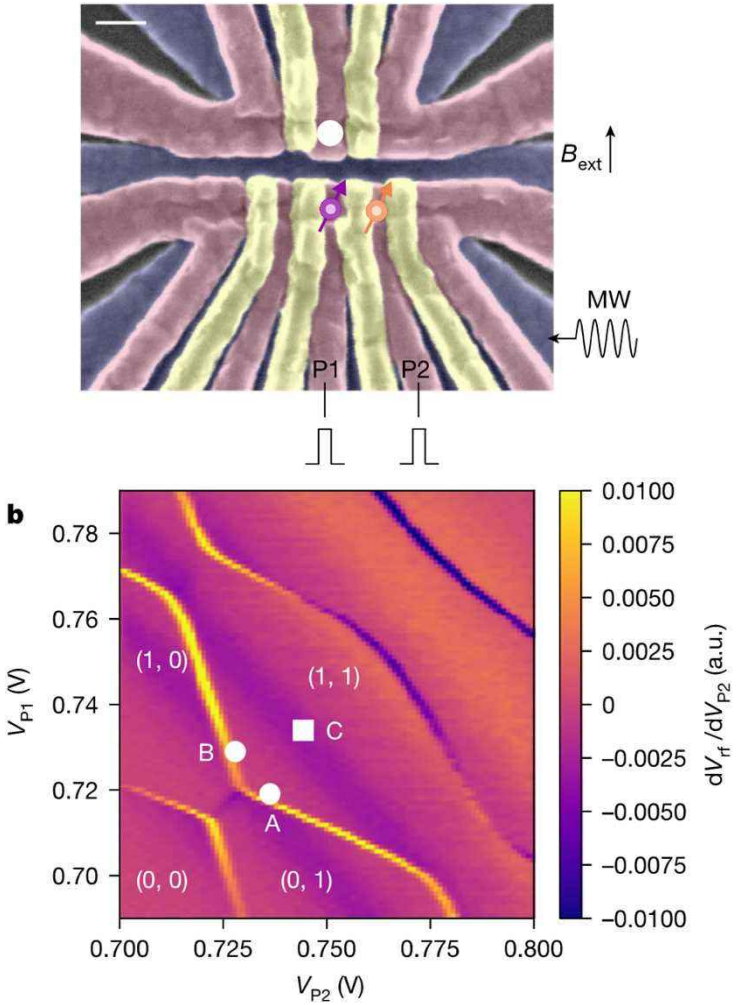
T. Utsugi et al., SSDM (2022)

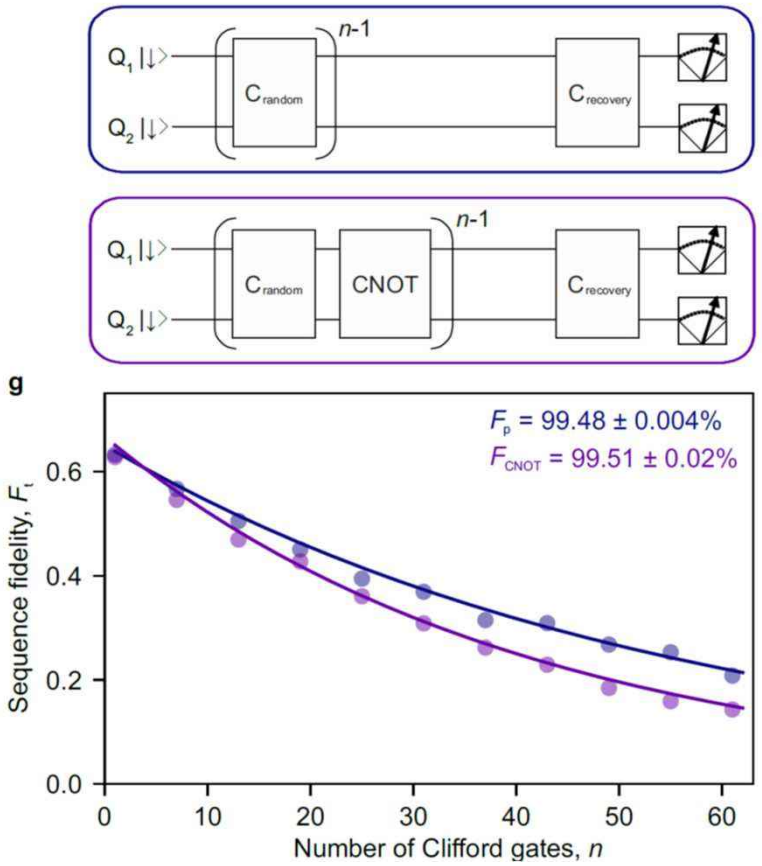
* S. P. Giblin et al., Metrologia 56, 044004 (2019).

Qubit operation in SiGe small qubit system (1)

■ First demonstration of high-fidelity 2-bit-gate operation above the error tolerance threshold (Simultaneously with QuTech et al.)

✓ **Successfully developed a qubit system that enables verification of high-fidelity qubit operations.**



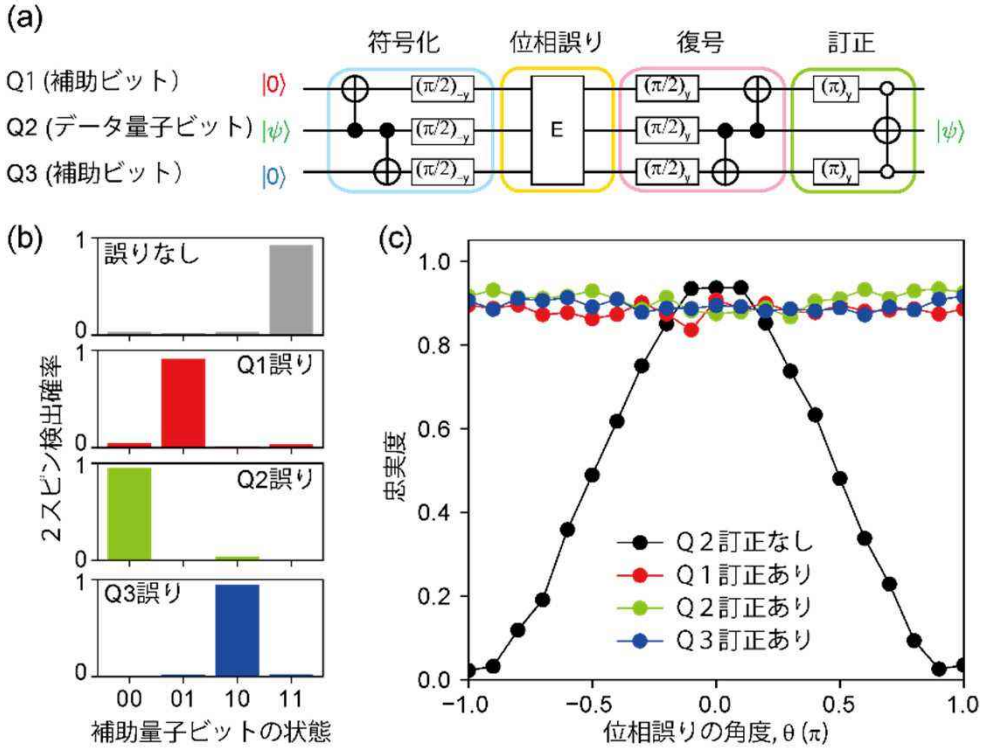


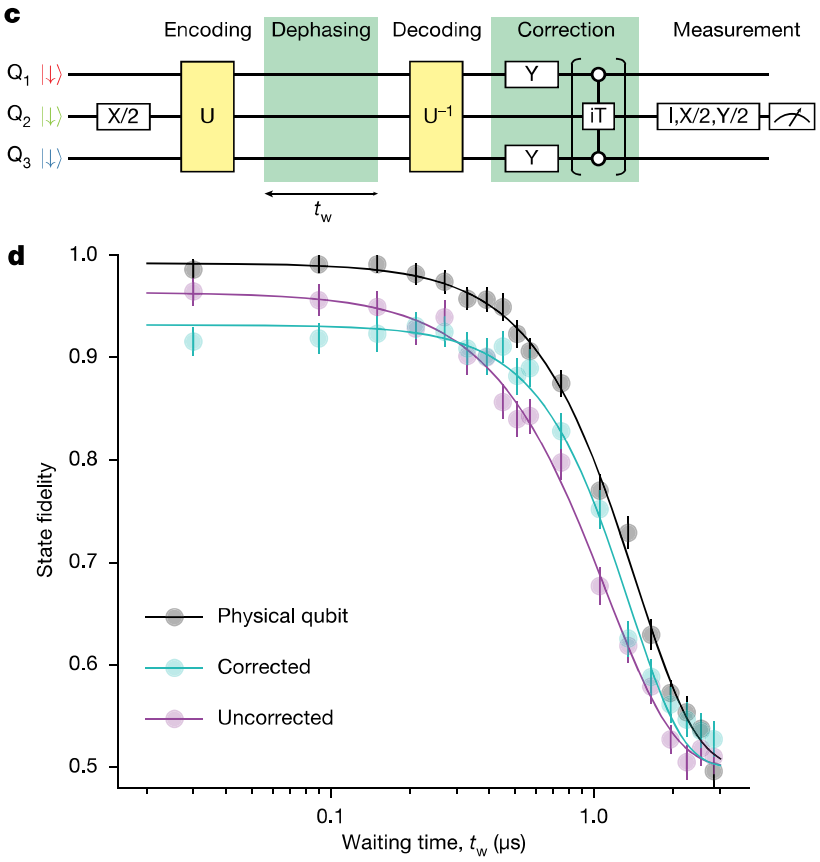
A. Noiri *et al.*, Nature **601**, 338 (2022)

Qubit operation in SiGe small qubit system (2)

■ Demonstrating the feasibility of achieving error tolerance with silicon qubit arrays

- ✓ Generates 3-qubit quantum entangled states (GHZ states)
- ✓ World's first demonstration of silicon phase error correction circuit



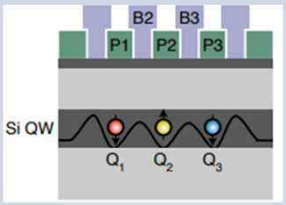
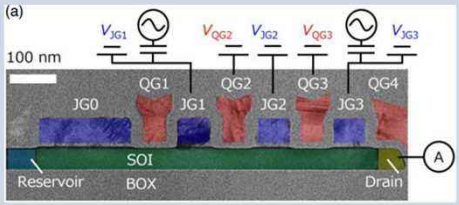


K. Takeda *et al.*, Nat. Nanotechnol. **16**, 969 (2021)

K. Takeda *et al.*, Nature **608**, 684 (2022)

Qubit operation in qubit array

- Remarkable progress has been made in small systems using SiGe qubits. However, it has been a challenge in qubit arrays using Si-MOS qubits.
- Theoretical studies and multiple device prototypes (using multiple fabs) are being proceeded in parallel.

	RIKEN / SiGe	This project / Si-MOS	Concerns resulting from differences
Device structure			
Basic properties	• Isotopic content: ^{29}Si 0.08%, ^{30}Si 0.00% • Mobility: 1.5×10^5 • Effective mass: 0.13	• Isotopic content: ^{29}Si 4.7%, ^{30}Si 3.1% • Mobility: 1.0×10^4 • Effective mass: 0.14	• Purified wafers can be introduced in the future
Confinement structure (Perpendicular direction)	• Well structure: SiGe 30nm / Si 8nm / SiGe 30nm	• Well structure: SiO_2 5nm / SOI 50nm / BOX 145nm	• Valley degeneracy/splitting • Charge in the gate
	• Gate material: Al/Al_2O_3	• Gate material: Poly-Si/SiO_2	
Confinement structure (In-plane direction)	• Si - SiGe surface	• SiO_2 - Si surface	• Surface roughness
	• Isolation: Field isolation	• Isolation: Shallow-Trench-Isolation (STI)	• Fixed charges/defects due to STI
	• Dimensions: Unknown	• Dimensions: 60 nm	• Multiple quantum dots
Spin operation system	• Spin operation: EDSR	• Spin operation: ESR	• Required RF power transfer has been confirmed by simulation
	• Local *B* generation: Micromagnets (Co/Ti)	• Local *B* generation: Local current	• Heat is the biggest concern, but not a problem in current simulation

Shuttling qubit operation

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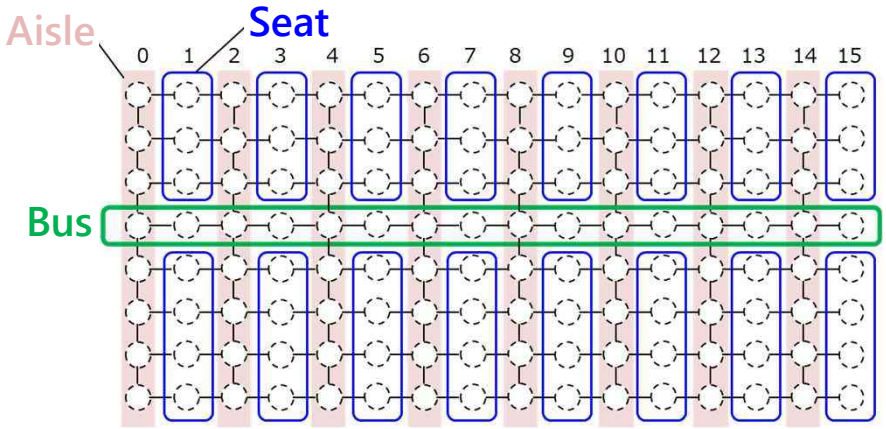
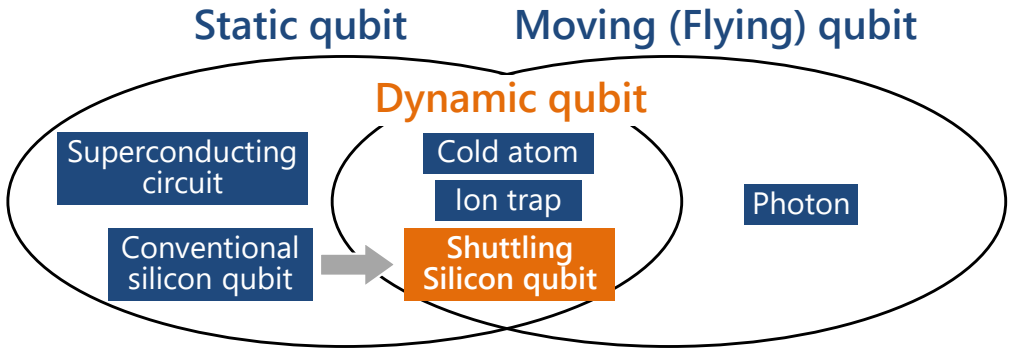
■ In addition to the operation of qubits in small systems, another concern is the operation of qubits in qubit array systems. Shuttling qubit separates the electron from the quantum dot, meaning that a “qubit” can move (shuttle).

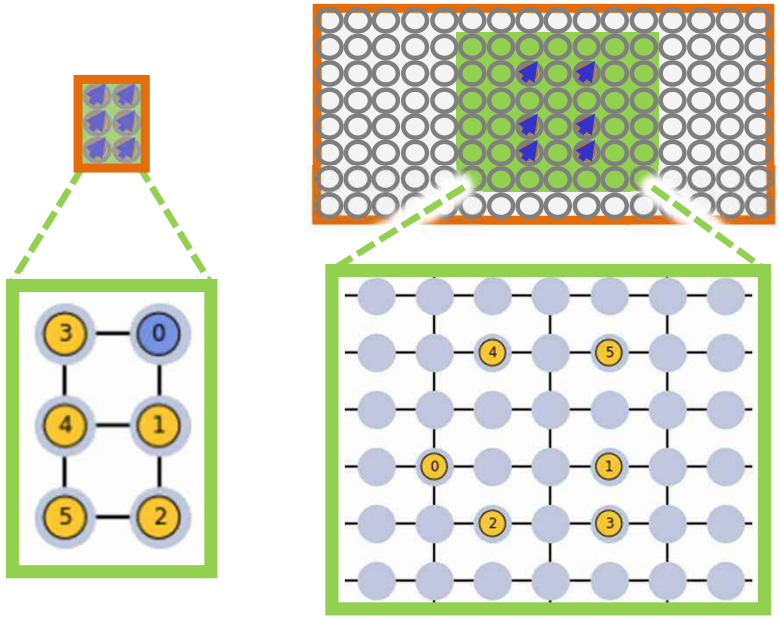
- ✓ Qubit array are divided into Bus/Aisle/Seat regions in order to dynamically rearrange qubit without congestion.
- ✓ It suppresses crosstalk and enables all-to-all connections among up to 56 qubits in a 16 x 8 qubit array.



- ✓ Shuttling qubits create a new categorization of qubits



- ✓ Shuttling qubits take advantage of silicon semiconductor technology and use quantum dots quite luxuriously.



Conventional Shuttling

Demonstration of 6-Qubit QAOA operation

Readout

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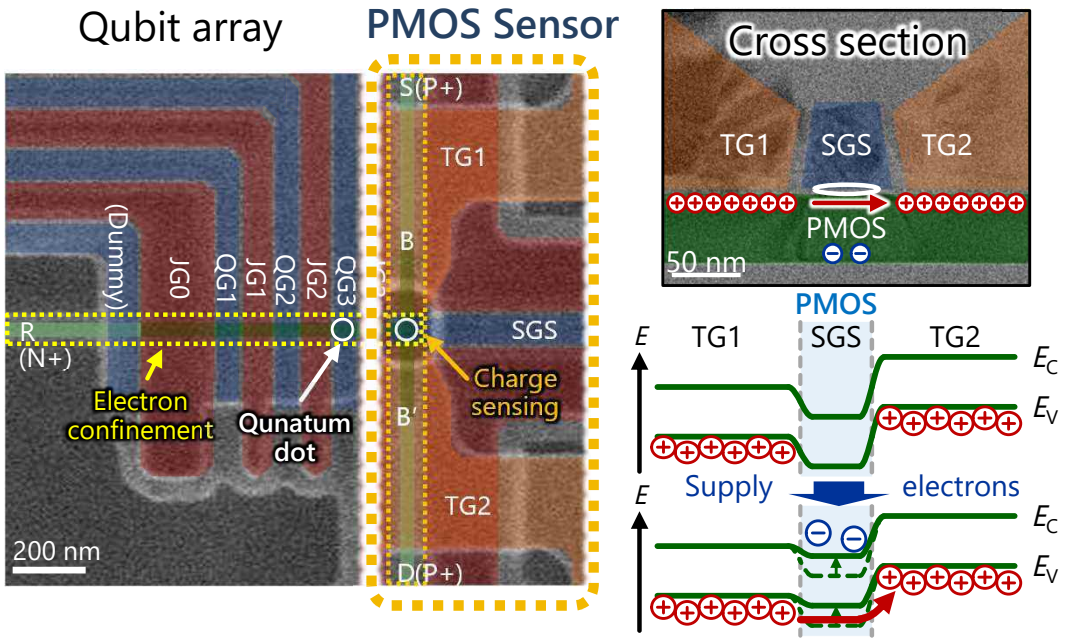
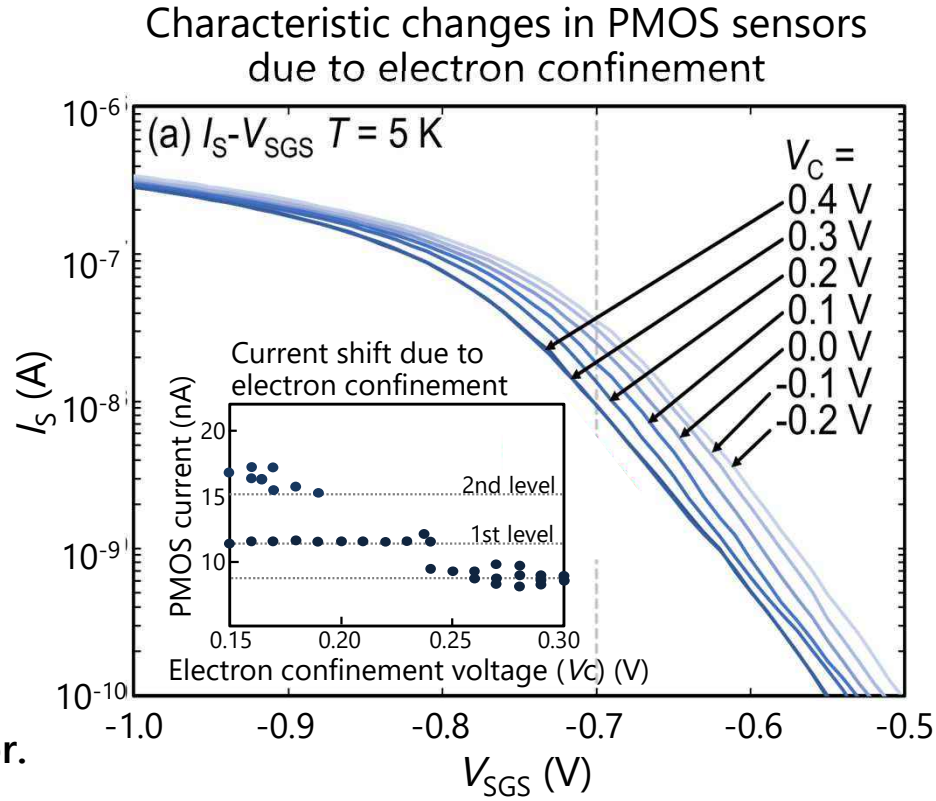
- High-frequency reflectometry measurement is widely used.
  Challenge is that it is difficult to support large-scale qubit integration.
- Developed a PMOS sensor capable of detecting a single electron.

✓ If the difference in the number of electrons can be converted into a current change of the order of nA, the sense amplifier circuit used in SRAM/DRAM becomes possible.





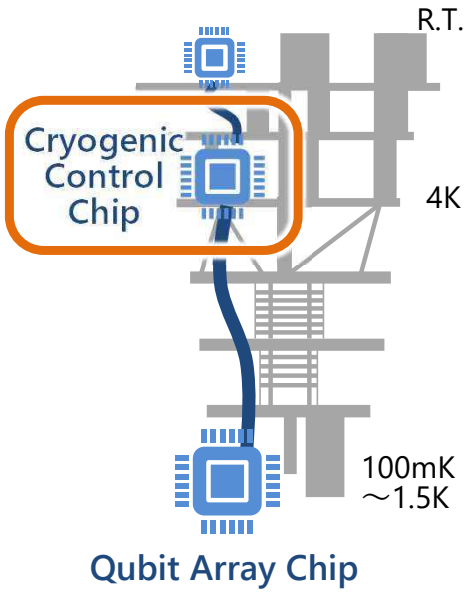
✓ Potential barrier in the channel region of the PMOS is lowered due to electron confinement to the PMOS sensor.

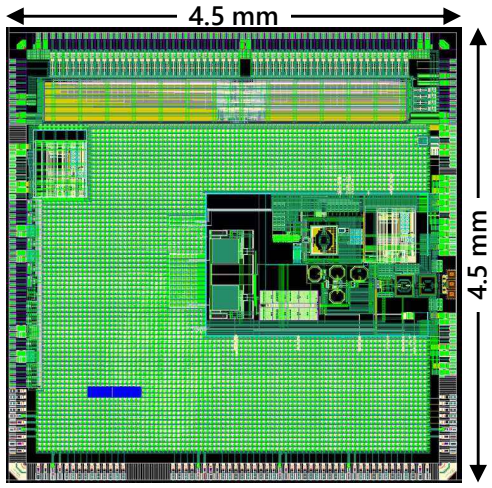
✓ This causes the current in the PMOS sensor to change on the order of nA.

D. Hisamoto et al., Applied Physics Express letter (2023)

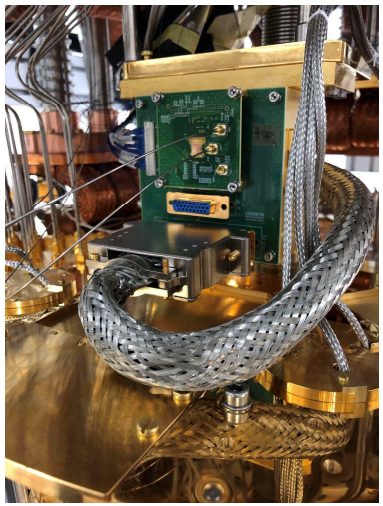
Cryogenic Control Chip (1)

■ 40-nm CMOS cryogenic control chip was developed and is evaluating.

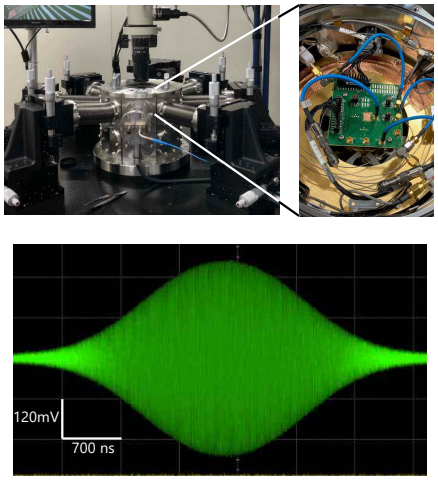




Cryogenic Control Chip



Implementation on 4K stage of dilution refrigerator



20 GHz Gaussian waveform

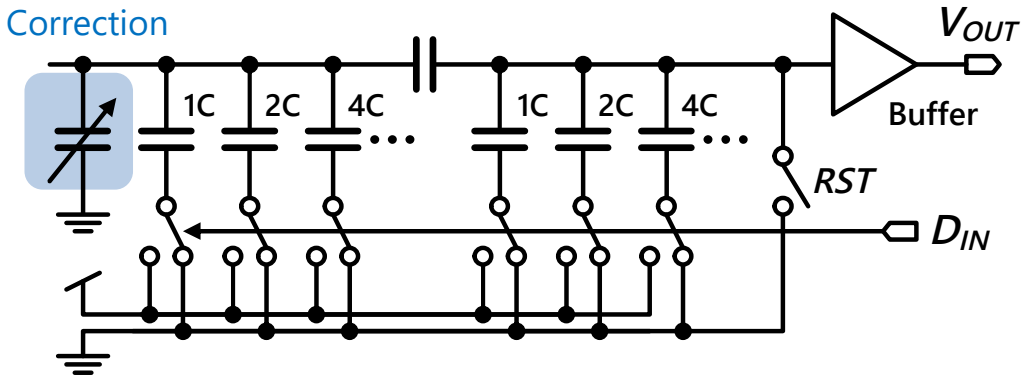
Circuit Blocks	Characteristics
(1) Timing Generator	• Timing Rage: 1 ns ~ 2 ms、Resolution: 1 ns
(2) Microwave Generator	• 20 GHz microwave signal including PLL & mixer – Arbitrary waveform shapes (including Gaussian waveform) – Pulse width: 0.1 ~ 10 μs, Step: 0.35° – Amplitude: -15 ~ 3 dBm – Phase error: <5.69° (Improved circuits under development)
(3) Bias Voltage Generator	• 59 Channels • Voltage range: 0 V ~ 2.5 V, Resolution: 16 bit (1 LSB = 40 μV)

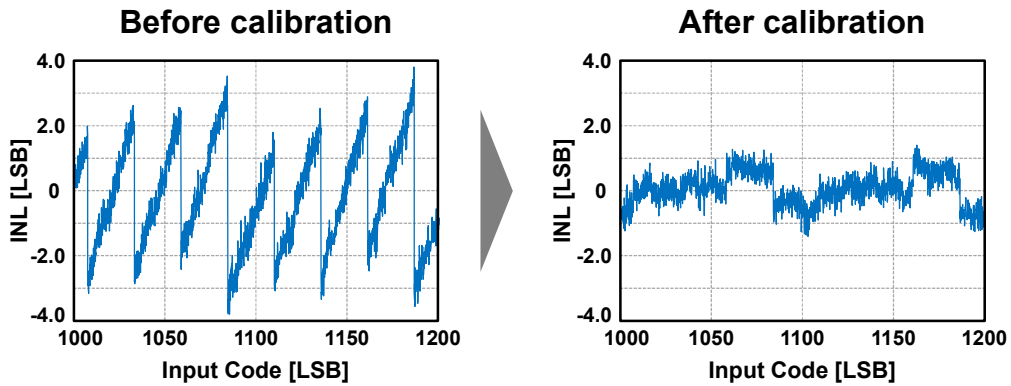
Cryogenic Control Chip (2)

■ Cryogenic CMOS circuit design enabled high-performance analog circuits.

● Cryo-DAC for Bias voltage generation

- ✓ 16 bits (40 μV/LSB)
- ✓ Small-size Low-power architecture
  0.02 mm^2/ch
- ✓ Linearity compensation (Patent pending)

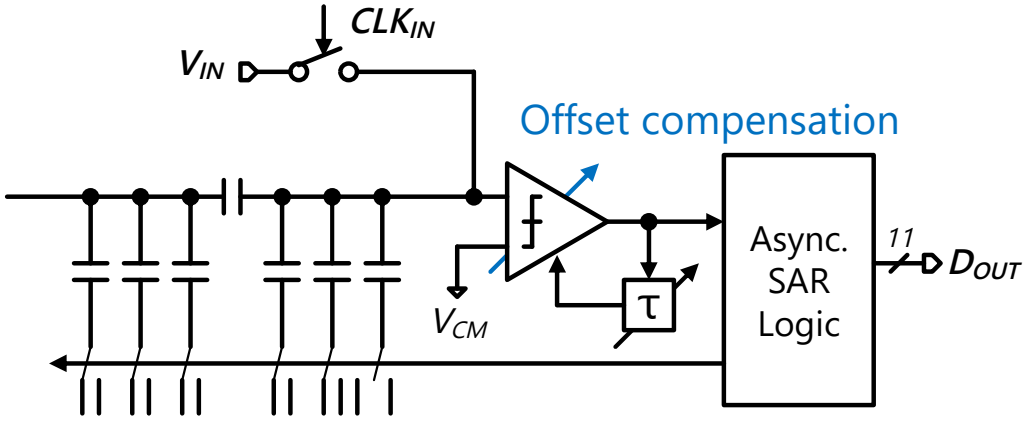


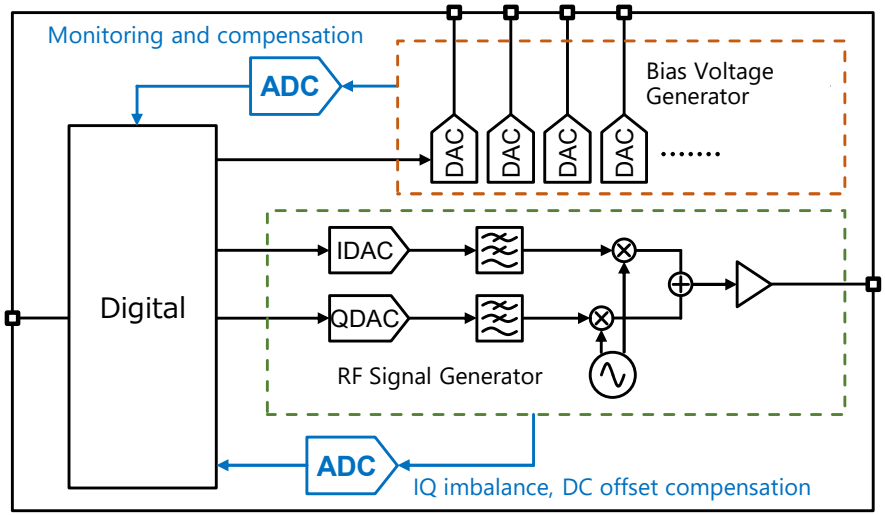


Miki, ASP-DAC 2023

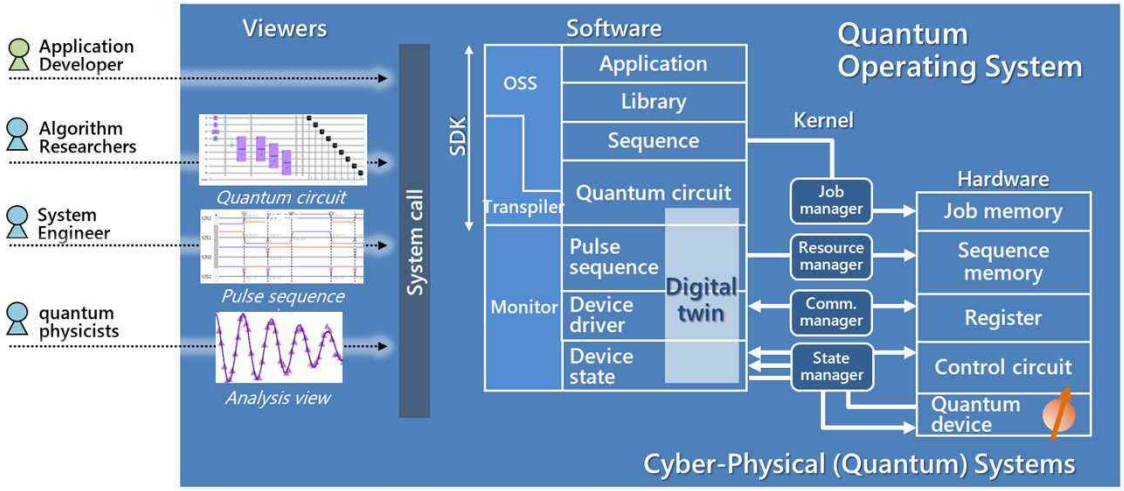
● Cryo-ADC for chip internal ckts compensation

- ✓ 11 bits, 100 MS/s
- ✓ Async. sequential comparison architecture
- ✓ Offset compensation



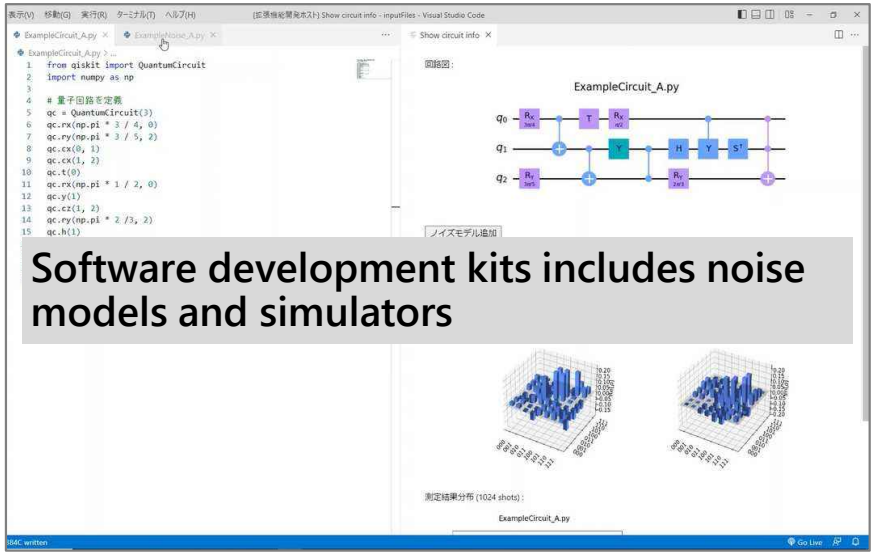


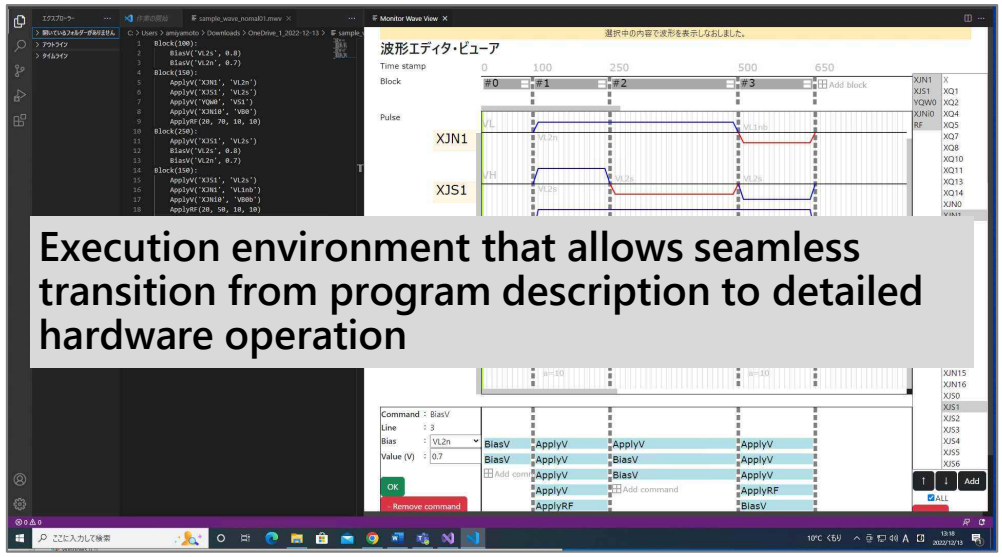
Quantum Operating System



SDK: Software Development Kit, OS: Operating Systems

- ✓ Quantum OS has a model (digital twin) of the qubits to be controlled and their operating environment to provides feedback control.
- ✓ Provide a multi-role usage environment for various users: quantum physics, quantum algorithm researchers, etc.

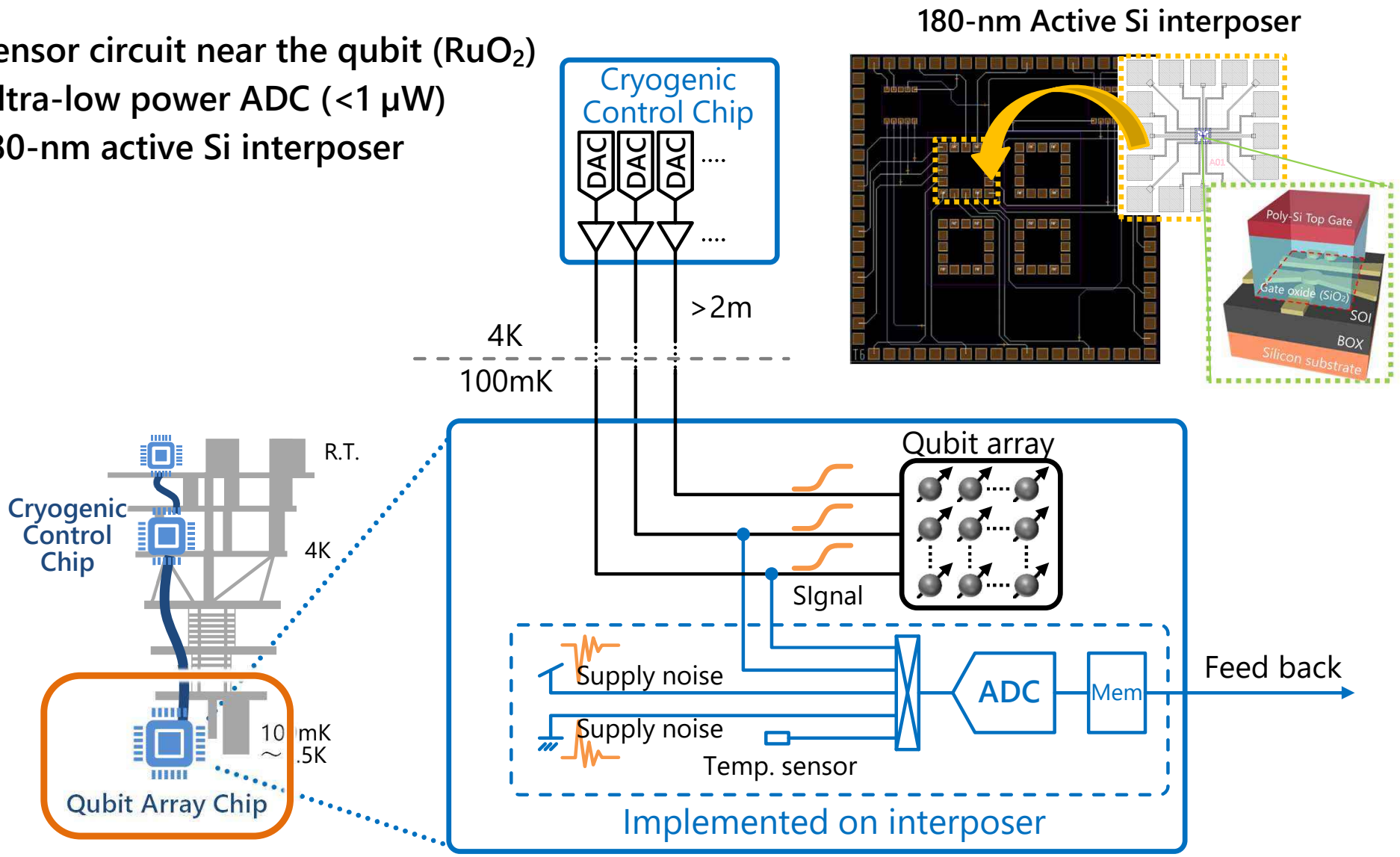




Environmental monitoring system

■ Monitor temperature and control signal waveforms that affect the fidelity of qubits

- ✓ Sensor circuit near the qubit (RuO_2)
- ✓ Ultra-low power ADC (<1 μW)
- ✓ 180-nm active Si interposer



Hot silicon qubits

■ Measurement of temp. dependence of noise to assess "hot operation" feasibility

✓ **We observed weak temperature dependence of charge noise in our silicon devices**

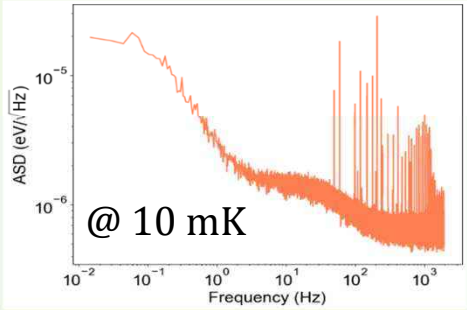
- **For electrons (in an n-type QD): $1/f$ component $\lesssim 1\ \mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$ @ 1 Hz up to ~1 K**
- **For holes (in a p-type QD): $1/f$ component $\lesssim 1\ \mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$ @ 1 Hz up to ~2 K**

cf. Charge noise level in few-electron SiGe QDs at 50 mK: $\lesssim 1\ \mu\mathrm{eV}/\sqrt{\mathrm{Hz}}$ @ 1 Hz

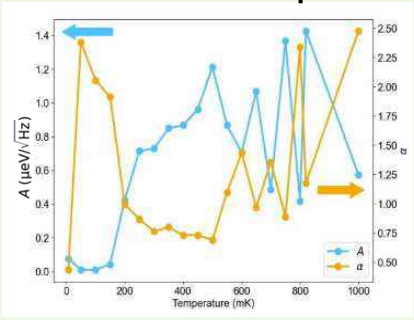
⇒ **Promise for hot silicon qubits**

Electrons

Amplitude spectral density of charge noise (potential noise)



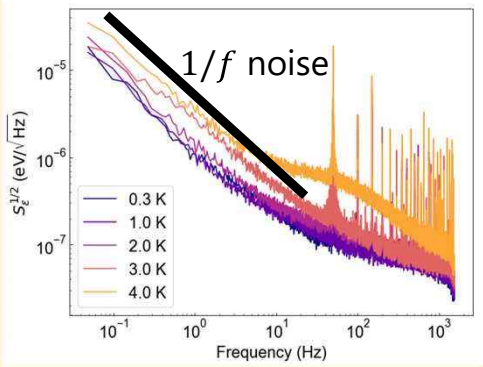
Temperature dependence of the $1/f$ noise component



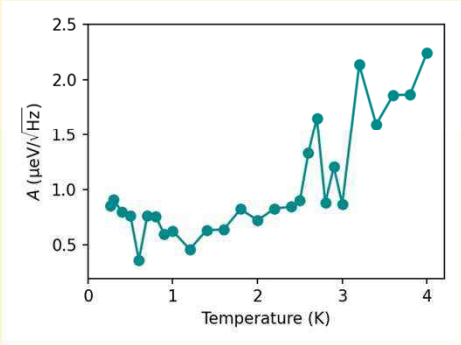
Arakawa et al., 70th Japan Society of Applied Physics Spring Meeting (2023).

Holes

Amplitude spectral density of charge noise (potential noise)



Temperature dependence of the $1/f$ noise component



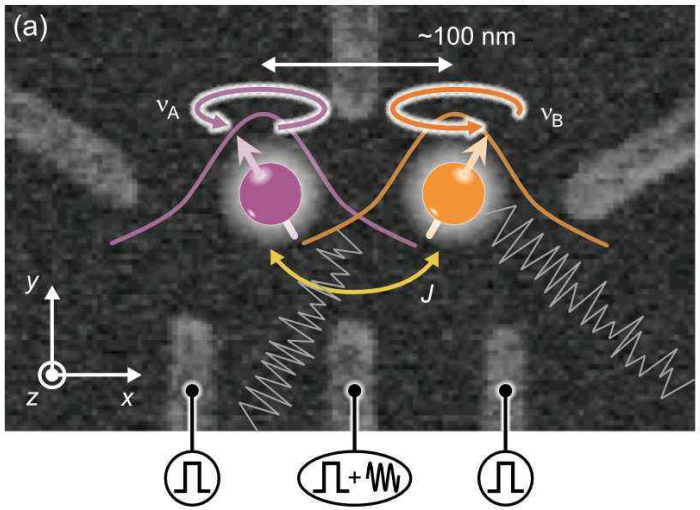
Nakagoe et al., 83rd Japan Society of Applied Physics Autumn Meeting (2022).

Nakagoe, Best Master's Thesis Award, Tokyo Tech (2023).

Error correlation of SiGe qubit arrays

■ Observed world's firstly the correlation of qubit phase noise

✓ Spatial correlation of qubit errors becomes apparent when qubits are arrayed, which is related to ease of error correction.



$$\mathcal{H} = \frac{h\nu_A}{2}\sigma_z^A + \frac{hJ}{4}\sigma_z^A\sigma_z^B + \frac{h\nu_B}{2}\sigma_z^B$$

Auto-correlation (Conv.)

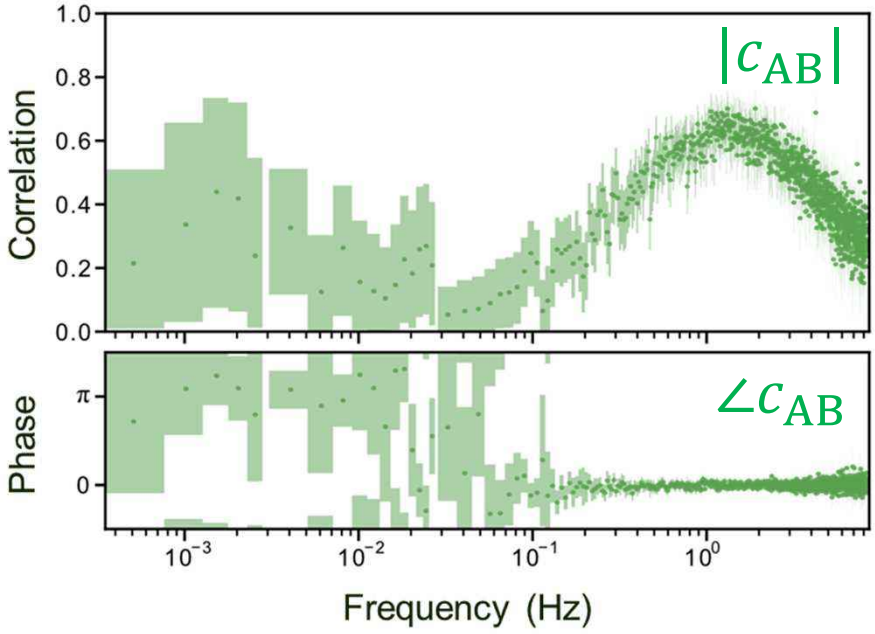
$$S_A = \mathcal{F}[\langle \nu_A(0)\nu_A(\tau)\rangle]$$
$$S_B = \mathcal{F}[\langle \nu_B(0)\nu_B(\tau)\rangle]$$

⇩ Cross-correlation

$$C_{AB} = \mathcal{F}[\langle \nu_A(0)\nu_B(\tau)\rangle]$$

Normalized

$$c_{AB} = \frac{C_{AB}}{\sqrt{S_A S_B}}$$



✓ Observed relatively large correlation of about 70%

✓ From anti-correlation to correlation
→ Depends on charge noise source spatial distribution

Summary

- Quantum computer R&D is shifting from a scientific curiosity phase to a technology development phase.
- I believe that for a quantum computer to have industrial value, it must be large scale in addition to be high fidelity. In this project, we're going to achieve a large-scale silicon quantum computer through a top-down approach in order to take full advantage of silicon semiconductor technology.
- In the past three years, we have developed several key technologies in addition to many remarkable research results.
- We will continue to demonstrate qubit operation in small systems, and at the same time, we will move forward with system integrations to achieve stable qubit operation and further improve the fidelity of qubit operation.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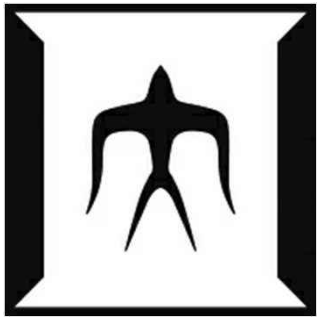


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