

Development of Superconducting Fault-Tolerant Quantum Computer Systems

Project manager

(selected in 2025)

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Leader's institution

National Institute of Advanced Industrial Science and Technology

R&D institutions

Kyocera Corporation, NanoBridge Semiconductor Inc., NTT Inc., ULVAC Inc., ULVAC Cryogenics Inc. Chuo University, Keio University, Kobe University, Kyushu University, Nagoya University, The University of Osaka, The University of Tokyo, Tohoku University, Tokyo University of Science, National Astronomical Observatory of Japan, National Institute of Advanced Industrial Science and Technology, National Institute of Information and Communications Technology, National Institutes of Natural Sciences, RIKEN

Summary of the project

To realize a practical fault-tolerant quantum computer, the number of physical qubits must be scaled up to roughly ten thousand times the current level. However, today's superconducting quantum computers have poor scalability to large systems, which has become a truly critical issue.

In superconducting quantum computers, each physical qubit requires its own dedicated circuitry for control and readout. At present, this means that from room-temperature electronics, at least one coaxial cable is connected for each physical qubit. This creates problems related to component space requirements and heat inflow through the coaxial cables—and as quantum computers grow larger, these issues become even more severe.

To drastically reduce the number of coaxial cables and maintain scalability that seems impossible through mere extensions of existing superconducting quantum-computer development, we propose a new architecture. In this architecture, room-temperature electronics are used only for controlling virtual logical qubits, while the systems that require wide-bandwidth communication—such as control, readout, and variation compensation for individual physical qubits—are consolidated into chipllets operating at cryogenic temperatures. We aim to take on the challenge of realizing this architecture in actual hardware.

What makes this possible are our digital-assisted analog circuit technologies using superconducting circuits and our three-dimensional wiring technologies. By creating compact chipllets capable of controlling, reading out, and correcting physical qubits entirely within an environment cooled to 10 mK, we will demonstrate system-level operation of a fault-tolerant quantum computer.

Milestone by the year 2030

We will develop a fault-tolerant quantum computing system equipped with a quantum processor that achieves uniformity and high density for more than 100 physical qubits. By operating error-correction functions based on the surface code on this system, we will demonstrate that logical qubit information can be preserved continuously, and at the same time, show that gate operations on logical qubits can be performed with a suppressed logical error rate.

Milestone by the year 2028

We will establish a path to solving one of the biggest factors limiting scalability: variations in the characteristics of physical qubits. We will fabricate a chip containing more than 50 physical qubits equipped with a frequency-tuning mechanism compatible with scalable architectures, and demonstrate that qubit frequency variations can be sufficiently suppressed after tuning.

Project structure

