Goal 6 Realization of a fault-tolerant universal quantum computer that will revolutionize economy, industry, and security by 2050.

Development of Fault-Tolerant Silicon Quantum Computing Technologies

Project manager

(selected in 2025)

TARUCHA Seigo

Group Director, RIKEN Center for Emergent Matter Science / Team Director, RIKEN Center for Quantum Computing

Leader's institution

RIKEN

R&D institutions

RIKEN
Kobe University
Hitachi, Ltd.
Institute of Science Tokyo
The University of Tokyo
The University of Osaka
AIST

Summary of the project

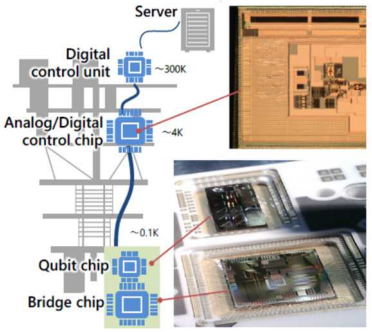
This project aims to develop scalable multi-qubit devices with error correction toward realization of fault-tolerant silicon quantum computers. We will apply qubit integration and qubit-shuttling technology to implement a unit structure of qubits and scale up the qubit devices by integrating the unit structures. We will establish technology bases appropriate to implement large-scale quantum computers by 2030, and expand them in cooperation with the semiconductor industry to realize fault-tolerant large-scale quantum computers by 2050.

Milestone by 2030

We will develop technologies for scalability and error correction that form the foundation for the realization of large-scale quantum computers in collaboration with industry. Furthermore, we will develop scalable interconnect and packaging technologies in pure Si/SiGe, along with core qubit technologies —such as qubit control, readout, coupling via qubit transfer, and high-quality qubit transfer channels—and integrate them into a coherent system.

Milestone by 2028

Using isotopically enriched Si/SiGe substrates, we will develop scalable multi-qubit device technologies that enable high-fidelity quantum operations, and on this basis fabricate unit structures for two-dimensional qubit arrays. Utilizing a portion of these structures, we will conduct proof-of-principle experiments on quantum error correction. In parallel, we will advance elemental qubit technologies compatible with large-scale multi-qubit integration.



Silicon quantum computing system

Project structure

Seigo TARUCHA (RIKEN)

Item 1 Control of integrated silicon spin qubits for fault-tolerant quantum computing
- 1-1 Development and control of integrated silicon spin qubits for fault-tolerant quantum computing (Takashi NAKAJIMA/ RIKEN)
- 1-2 Development of scalable interconnect technologies for silicon qubit systems (Takuji MIKI/ Kobe University)

Item 2 Prototyping of fault-tolerant qubit devices and system integration
- 2-1 Development of prototype of fault-tolerant qubit devices and system integration (Hiroyuki MIZUNO/ Hitachi, Ltd.)

Item 3 Scalable foundational technologies
- 3-1 Development of scalable qubit readout technologies (Tetsuo KODERA/ Institute of Science Tokyo)
- 3-2 Development of scalable qubit drive technologies (Jun YONEDA/ The University of Tokyo)
- 3-3 Development of middle-distance quantum link (Takafumi FUJITA/ The University of Osaka)
- 3-4 Development of isotopically engineered Si/SiGe substrate and device integration technologies (Satoru MIYAMOTO/AIST)

JST Japan Science and Technology Agency