Goal 6 Realization of a fault-tolerant universal quantum computer that will revolutionize economy, industry, and security by 2050.

Here begins our new MIRAI
MOONSHOT RESEARCH & DEVELOPMENT PROGRAM

Development of a Scalable, Highly Integrated Quantum Error Correction System

Project manager

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R&D institutions

Kyoto Institute of Technology, University of Tokyo, Kumamoto University, Osaka University, Kyoto University, University of Shiga Prefecture, RIKEN, High Energy Accelerator Research Organization , Meiji University, Toyama Prefectural University, QuEL Corporation, Socionext Inc.

QUBECS
Quantum Bit Error Correction System
Moonshot Target 6

Summary of the project

To realize an error-tolerant general-purpose quantum computer, this project addresses the technical issues of algorithms and scalable backends by using classical hardware for error correction, scalable quantum-to-classical input/output frontends, their chip implementation, and cryogenic operation for high bandwidth and low power quantum-to-classical input/output. We will address the technology challenges of optical integrated circuits. This will enable error correction systems for general-purpose quantum computers that can be used universally by 2050 through error correction.

2025 (3year) — Development of a prototype quantum error correction

- Error correction on the backend alone
- Smaller & more power efficient front end
- Operation check of a stand-alone optical-Cryo interface
- Operation check of stand-alone circuit for Cryo Qubit control

2030 (8year) — Scalable and practical quantum error correction process feasibility

- Coordinated operation of backend and frontend
- Establishing backend scalability
- Completion of optical-Cryo CMOS interface
- Completion of Cryo Qubit-controlled SoC

2050 — Development of a Scalable, Highly Integrated Quantum Error Correction System

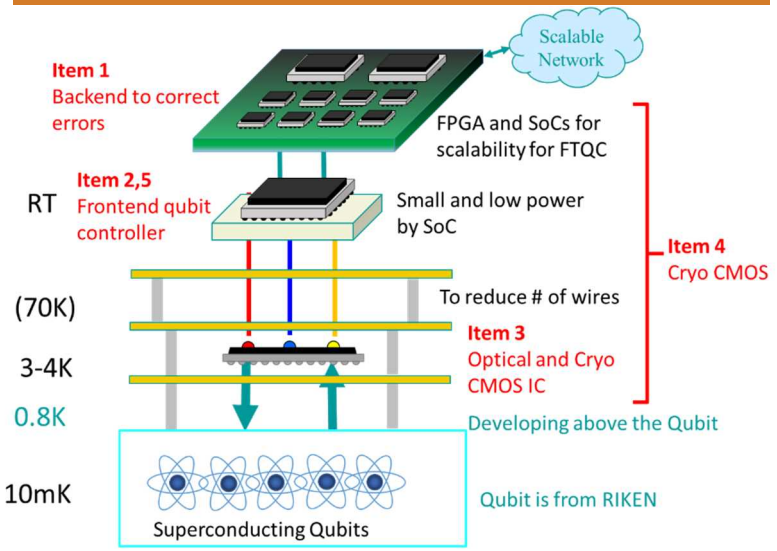
Milestone by year 2030

We will demonstrate the feasibility of scalable and practical quantum error correction processing.

Milestone by year 2025

We will develop a prototype of a quantum error correction system and integrate the qubit control part to make it smaller.

R&D theme structure of the project



		R&D item	Performer
1	**Backend for error correction**		
	1	Scalable backend system for error correction	Sano (Riken)
	2	ASIC implementation of QEC cores	Kadomoto (U Tokyo)
	3	Dependable error correction backend	Osana (Kumamoto U)
2	**Adovanced Qubit Control Frontend**		
	1	Advanced Qubit Control Frontend	Miyoshi (Quel)
3	**Scalable Classical-Quantum Interface by Photonic/Cryo-CMOS Integrated Circuits**		
	1	Exploring photonic integrated circuits operating in the extremely low-temperature environment	Shiomi (Osaka U)
	2	Construction of Cryo-CMOS PDK	Shintani (KIT)
	3	Cryo-CMOS integrated circuit design infrastructure	Sato (Kyoto U)
4	**Cryo CMOS ASICs for Frontend/backend**		
	1	Digital circuit implementation and reliability enhancement techniques	Kobayashi (KIT)
	2	RF frontend circuit	Tsuchiya (U Siga Pref.)
	3	High-speed DAC for frontend	Takai (KIT)
	4	High-speed ADC for frontend	Miyahara (KEK)
	5	RTL design of digital circuits for frontend	Imagawa (Meiji U)
	6	Layout design of digital circuits for frontend	Kishida (Toyama Pref. U)
5	**Frontend Analog RF LSI at Room Temperature**		
	1	Frontend Analog RF LSI at Room Temperature	Igarashi (Socionext)

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