

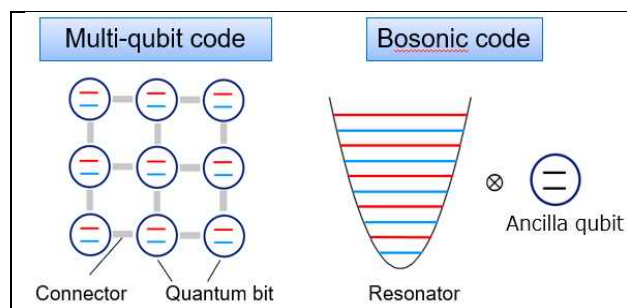
R&D Theme Name

Research and development of qubit circuits for error tolerant quantum computers

Progress by FY2022

1. Overview

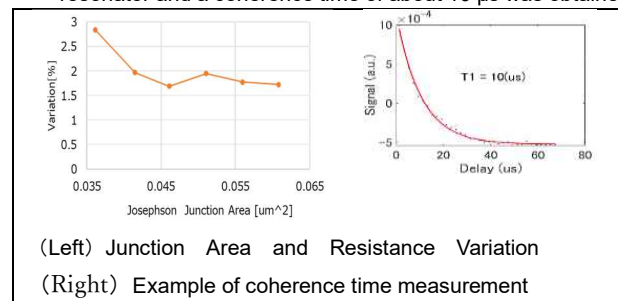
One of the hardware challenges in realizing an error-tolerant general-purpose quantum computer is that a large number of physical qubits are required to implement error-correcting codes, and in the case of superconducting qubits, the number is said to be enormous (10^8) at typical error rates ($\sim 0.1\%$). To solve this problem, this R&D theme will contribute to reducing the number of qubits required to realize an error-resistant general-purpose quantum computer by investigating the causes of errors and developing high-quality qubit manufacturing technology based on this research. In addition, since current manufacturing methods (Electron beam exposure and oblique deposition methods) present challenges in terms of productivity and qubit uniformity for future large-scale circuits, we will develop qubit fabrication technology using optical exposure and stacking processes. We will also conduct exploratory research on bosonic codes, which are expected to enable error-resistant quantum computation with fewer physical qubits than the currently mainstream surface codes, to identify the possibilities and promising schemes. We will also conduct exploratory research on bosonic codes, which are expected to enable error-resistant quantum computation with fewer physical qubits than the currently mainstream surface codes, to identify the possibilities and promising schemes.



2. Results by FY2022

① Development of large-area, high-throughput Josephson junction fabrication technology

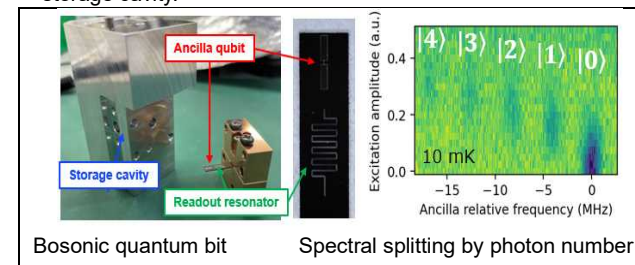
Current fabrication of superconducting quantum circuits is typically done using electron beam lithography and angle deposition. However, as circuits become larger in scale and wafers become larger in diameter, the current method poses problems in terms of manufacturing throughput and qubit fabrication variability. To solve these problems, we are developing a superconducting qubit circuit fabrication process that is compatible with state-of-the-art semiconductor processes using 300 mm wafers. This time, qubits were fabricated using optical exposure (ArF immersion) for patterning. The 2% resistance variation at room temperature was achieved for a Josephson junction of the same size as the qubit. The fabricated qubits were evaluated using a 3D resonator and a coherence time of about $10 \mu\text{s}$ was obtained.



② Research and development of bosonic cords using superconducting resonators

Error-correcting codes, called bosonic codes, are a method of protecting quantum information from errors by utilizing the degrees of freedom of the energy levels of resonators, which are in principle infinite, and are expected to reduce the number of physical qubits actually required as hardware compared to conventional methods. By the previous fiscal year, Q values exceeding the eighth power of 10 had been obtained in the prototype 3D (cavity) resonator, which were equal to or better than those of the previous study. This year, we optimized the design of bosonic qubits and improved the characteristics of ancilla qubits. By improving the design and fabrication method

of ancilla qubits, we were able to achieve coherence times of tens of microseconds with good reproducibility, creating an environment in which bosonic qubits can be implemented. As a first step, we have successfully observed the spectral splitting of auxiliary qubits according to the number of photons in the storage cavity.



3. Future Directions

Regarding the development of a large-area, high-throughput Josephson junction fabrication technology, we aim to establish a fabrication method for qubits that does not use angle deposition. In parallel, we will work on reducing the variation of qubits and improving the coherence time. For the bosonic code, we will implement the binominal code in the resulting resonator, and in parallel, we will proceed with a prototype niobium resonator to achieve an even higher Q-value.

R&D Theme Name

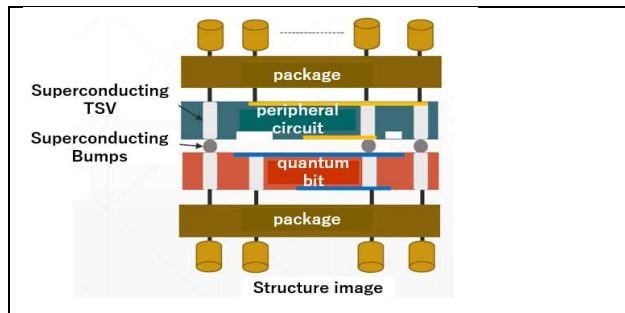
Research and development of qubit-integrated hardware systems

Progress by FY2022

1. Overview

In the typical setup of today's superconducting qubit circuits, qubit chips placed at cryogenic temperatures and microwave electronics operating at room temperature are wired together by one or more coaxial cables per qubit. However, this method cannot scale up to tens of thousands of qubits or more due to the limitations of space and cooling capacity of the cryocooler. To solve this problem, this R&D theme aims to develop hardware technologies around quantum chips, such as a high-capacity dilution refrigerator with high cooling capacity and connector-less high-density wiring, to break through the wiring bottleneck for integration.

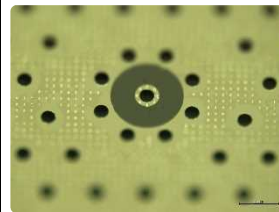
The key to this development is how to control and process signals in the vicinity of the qubits and reduce wiring between different temperature stages. For this purpose, we are developing a "vertically integrated" qubit module, in which a qubit chip is hybrid-integrated with a signal processing circuit that controls and reads out the qubits. For the dilution refrigerator, we are optimizing the entire refrigerator system, including not only the 10mK stage where the qubit chips are placed, but also the high temperature stage where the cryoelectronics may be placed.



2. Results by FY2022

1) Development of Transparent Mounting Structure

Design, prototyping, and evaluation experiments are underway to realize a vertical transmission-type mounting module structure as an electrical connection for vertically stacked structures. Specifically, we are working on technology to create an intra-board coaxial structure using through-substrate vias (TSVs), technology to create micro indium solder bumps for inter-board connection, and technology to create superconducting electrodes as the connection technology between the top and bottom surfaces of the boards. First, we developed a prototype chip for evaluation of stacked chips, and then developed a flip chip bonding technology for stacking three chips with six layers (assuming a qubit substrate, readout substrate, and upper wiring substrate). We continued with the design and fabrication of a vertical input/output package to house the vertically transparent mounting module with such stacked chips, as well as the fabrication of a magnetic shielding. In addition, to evaluate low-temperature electrical characteristics, we installed a refrigerator and electrical characteristics measurement equipment.



Test chip for vertical transmission module



Package of module mounted on a refrigerator

(2) Design of high-power dilution refrigerator

In order to scale up quantum computers, increasing the refrigeration power is needed in the millikelvin [Supplement 1] range of dilution chillers. In FY2022, based on the results of the previous year, we have worked to improve the efficiency of the heat exchanger, which is a key component, in order to achieve higher

output, and have obtained results that are expected to improve the refrigeration capacity.



Dilution refrigerator under prototype

[Supplement 1] A Kelvin is a unit of temperature that is zero at absolute zero (-273.15°C). mK (millikelvin) is 1/1000 of Kelvin. mK (millikelvin) is 1/1000 of mK. Since superconducting qubits require a cryogenic temperature of about 10 mK (-273.14°C) to operate, dilution refrigerators are used.

3. Future Developments

Regarding the transmission-type mounting structure, we will prepare an evaluation environment for the prototype vertical transmission-type mounting module and proceed with high-frequency electrical characteristics evaluation experiments, such as transmission loss and resonator characteristics.

With regard to the dilution refrigerator, the challenges to realize an error-tolerant general-purpose quantum computer are to further increase the cooling power and to optimize the cooling power at each temperature stage. We will conduct research and development to further increase the cooling power to 1.3 mW from the 0.97 mW at 100 mK achieved so far.

R&D Theme Name

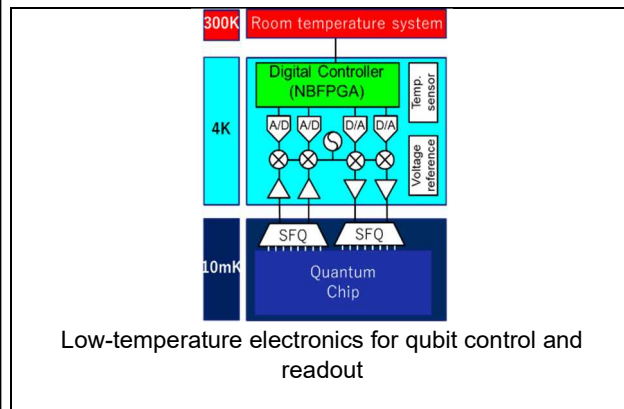
Research and development of electronics for quantum error correction

Progress by FY2022

1. Overview

In the typical setup of today's superconducting qubit circuits, a qubit chip placed at cryogenic temperatures and microwave electronics operating at room temperature is wired together by one or more coaxial cables per qubit. However, due to limitations in space and cooling capacity of the refrigerator, this method cannot handle the scale-up of qubits. To solve this problem, this R&D theme aims to develop qubit control and readout electronics that operate as close to the qubit as possible and to break through the wiring bottleneck for integration. In this development, the challenge is how to realize a control system that efficiently performs quantum error correction within the limited space and cooling capacity of a refrigerator.

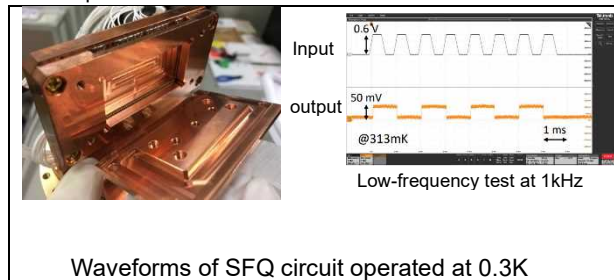
This R&D theme focuses on single flux quantum circuits, which can operate at several tens of GHz and have ultra-low power consumption, and atomic-switched FPGAs, which are highly flexible, capable of advanced processing, and have low power consumption, to develop low-temperature electronics systems in which they work together.



2. Results by FY2022

① Successful operation of a single flux quantum circuit using a low critical current density process

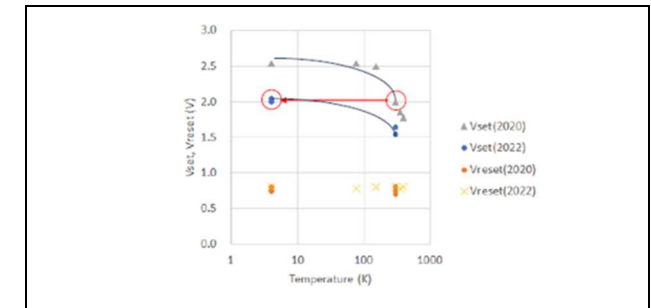
Single flux quantum (SFQ) circuits have been designed primarily for operation at 4 K. However, this research and development requires operation at 10 mK, which is the same as that of a qubit, and requires further reduction in power consumption of conventional SFQ circuits. Therefore, we are designing devices and fabricating chip prototypes with the aim of "reducing the critical current values of the Josephson junctions of the SFQ circuits to 1/10 or less," which is necessary for ultra-low power consumption. Last year, we tested the operation of a signal transmission circuit with the reduced power consumption of 1/50 at liquid helium temperature (4.2 K) on a prototype chip and obtained the expected signal at low speed. At lower temperatures, changes in device characteristics must also be considered. This year, we prepared an evaluation environment at 0.3 K and confirmed circuit operation at that temperature.



② Confirmation of rewrite operation at 4 K for a stand-alone nanobridge

We are developing FPGAs that can operate at low temperatures to support a variety of correction algorithms for error correction processing. FPGAs are designed to operate at 4 K. This research project is centered on developing an atom switch (NanoBridge) FPGA that can operate at low temperatures, which consumes 1/4 the power at room temperature compared to commercially available CMOS-based FPGAs. By last fiscal year, we had fabricated a prototype NanoBridge using a standard CMOS process (65 nm) and confirmed its programming at 4K. This fiscal

year, we succeeded in reducing the programming at 4K to the same level as that at room temperature by improving the manufacturing process. We also completed the circuit design of a NanoBridge FPGA for 4K operation using a process design kit for low-temperature, which was developed last fiscal year.



Reduced programming voltage of NanoBridge at 4K

3 Future Developments

For SFQ circuits, we will build a design library using various parameters extracted at cryogenic temperatures through prototype evaluation and proceed to design circuits such as qubit control signal demultiplexers. For nanobridges, based on the established design guidelines, we will specifically begin manufacturing NanoBridge FPGAs and fabricate chips.