Goal 6 Realization of a fault-tolerant universal quantum computer that will revolutionize economy, industry, and security by 2050.

Development of Integration Technologies for Superconducting Quantum Circuits

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R&D institutions

ULVAC Corporation, ULVAC Cryo Corporation, Osaka University, Kyushu University, Keio University, National Institute of Advanced Industrial Science and Technology, National Institutes of Natural Sciences, National Astronomical Observatory of Japan, National Institute of Information and Communications Technology, Tokyo Medical and Dental University, The University of Tokyo, Tohoku University, Tokyo University of Science, Nagoya University, NanoBridge Semiconductor Inc., Nikon Corporation, NEC Corporation, NTT Ltd., RIKEN

Summary of the project

To accelerate the research and development of superconducting quantum computers, we will develop elemental hardware technologies required for large-scale and highly integrated superconducting qubits. Thereby, we aim to realize a large-scale superconducting quantum computer by 2050.

To further scale up the ~100-qubit circuits currently developed around the world, the problem of the explosive increase in the number of wiring between the qubit chip and the control electronics must be solved. In this project, we aim to solve this problem by using cryoelectronics technologies such as single-flux quantum circuits and high-density wiring technology using flip-chip mounting.

In addition, to reduce the hardware requirements for realizing a quantum computer, such as the number of physical qubits and the number of wirings, we will develop high-coherence qubits and implement a new quantum error-correcting code called a bosonic code.

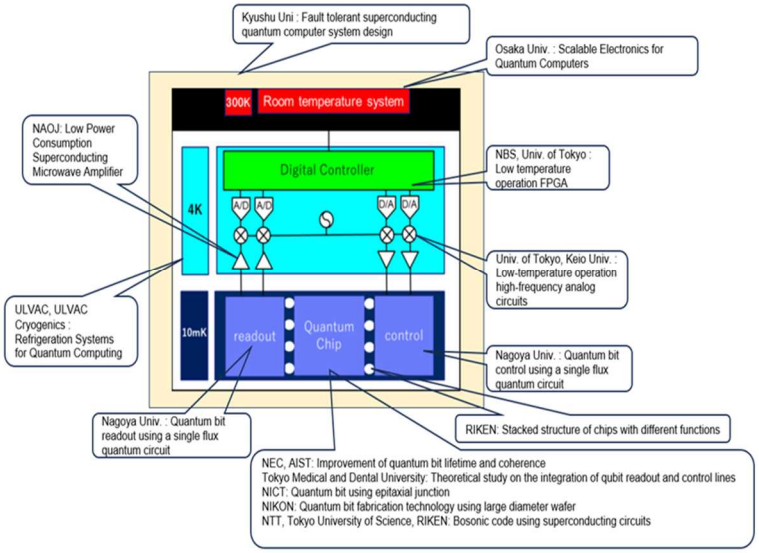
Milestone by the year 2030

Realizing quantum error correction using a method that can be applicable to the large-scale integration. The achievement of this milestone demonstrates the feasibility of quantum error correction at low temperatures and establishes a basic road map for the next decade to integrate large-scale qubits based on a basic stacked structure of qubit chips and classical circuit chips for qubit control and readout.

Milestone by the year 2025

We will realize low-temperature operation of the peripheral circuits and show the possibility of large-scale integration of superconducting qubits on a scale required for the error correction. The achievement of this milestone demonstrates that cryoelectronics can be used to control qubits with high precision.
This will lead to the next step of qubit readout using cryoelectronics and the stacking of qubit chips with classical circuit chips including cryoelectronics.

R&D framework of the project



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