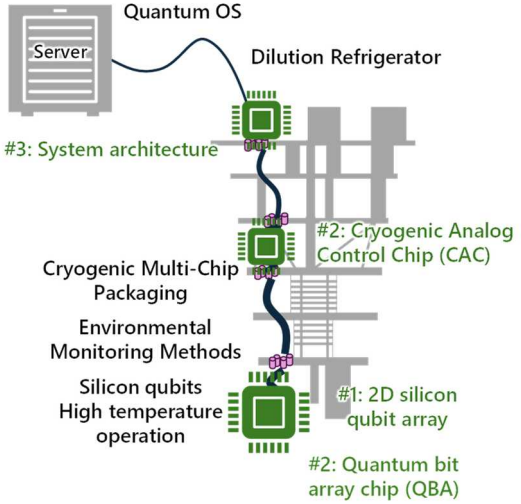
R&D Item

1. Quantum Computing System

Progress until FY2024

1. Outline of the project

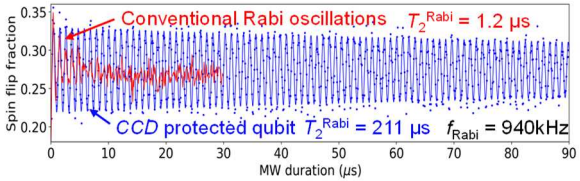
The R&D Item is responsible for overseeing the entire project and organising the quantum computer as a system and is working on three specific R&D tasks (#1, #2 and #3) in the diagram below. The first is research on the development of a two-dimensional qubit array of qubits, which is a milestone in the process of scaling up silicon quantum computers. The second is the development of qubit high-precision control and high-sensitivity readout circuits, which are necessary to control this qubit array with high precision and read out quantum information with high sensitivity. The third is to develop the system architecture for operating the entire system as a computer. Through these efforts, we aim to realise a large-scale integrated silicon quantum computing system that utilises the features of silicon semiconductor technology.



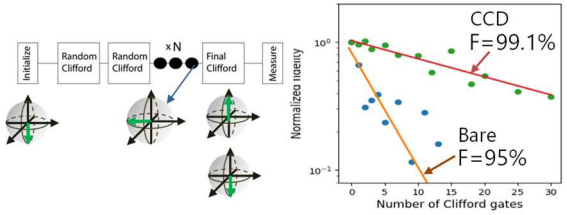
2. Outcome so far

In a study on two-dimensional qubit arraying, spin manipulation of one and two qubits was carried out through prototyping and evaluation of array structures. Spin manipulation sequences that further improve coherence in spin manipulation were investigated. In spin qubits, a qubit manipulation technique (Concatenated Continuous Driving: CCD) was developed to reduce external noise and extend the coherence time. CROT (Controlled-Rotation) spectra reflecting the entangled state of the two-qubit were observed, and a CROT-based two-qubit manipulation was successfully achieved.

- One-qubit spin operation (*CCD: Concatenated Continuous Driving) Confirmed life extension effect More than 100 times faster than before from 1.2 to 211 micro seconds.

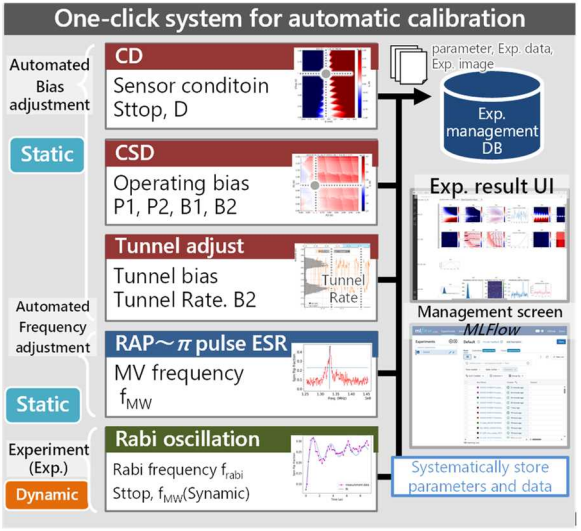


- High fidelity (99.1%) with Randomized Benchmarking



In the research on qubit high-precision control and high-sensitivity readout circuits, the detailed design of a microwave generator circuit chip applying the Polar modulation method, a phase reduction method, was completed for further high-precision control of qubits, and power efficiency was improved by operating the amplitude modulation intermittently and the LO (Local Oscillator) block for phase modulation. The sampling PLL (Phase-Lock-Loop) method was adopted for the LO block for phase modulation to reduce the phase. As a result of the study, the jitter, which is a phase error component, was expected to be reduced from 137 fsec to 80 fsec.

In the system architecture study, the quantum operating system was extended to assist the experimentalist and a one-click qubit measurement system was developed to automate single-qubit Rabi oscillation measurements. Methods to automate the analysis process were investigated and the implementation of an automated calibration library was completed. Demonstration tests using natural silicon devices confirmed that automatic calibration can reduce the measurement time by 81%, as well as ensuring traceability of the operating state and confirming the automatic calibration functionality against temperature and device characteristic fluctuations.



3. Future plans

Various innovations outside the norm are needed to realise FTQC. In collaboration with others inside and outside the project, we will realise qubit manipulation in a qubit array structure that makes maximum use of semiconductor technology, and furthermore work to improve the reliability and efficiency of such operations through system-level implementation.

R&D Item

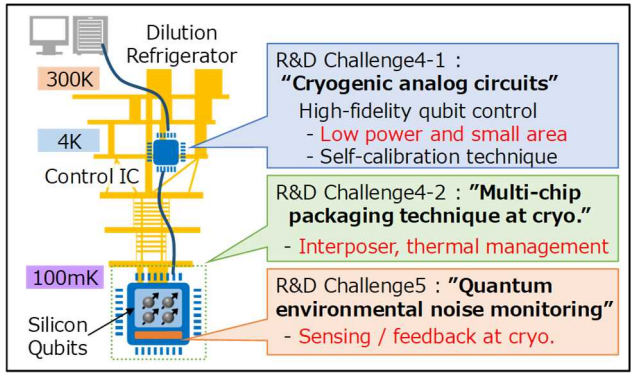
2. Multi-chip cryogenic packaging technology

Progress until FY2024

1. Outline of the project

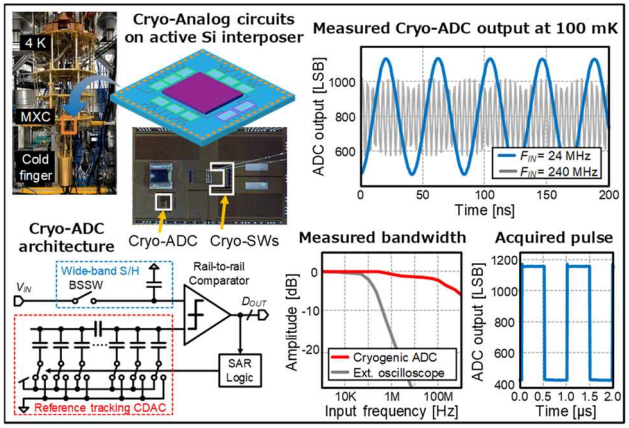
The main R&D Item of this project is to develop cryogenic circuits and implementation techniques for large-scale silicon quantum computers. This enables high-fidelity control and high-density implementation of a large number of silicon qubits, thereby contributing to the realization of error-tolerant quantum computers for Moonshot Goal 6.

In order to achieve this, we are tackling the following three challenging themes. First, we are developing ultra-small, low-power cryogenic analog circuits which enable control of numerous qubits inside a dilution refrigerator. Second, we are creating innovative packaging by integrating qubit chips and their interface functionality on an interposer to accommodate large-scale qubits within the refrigerator. Furthermore, we are establishing a monitoring technique that observes quantum environmental noise affecting the accuracy of qubits and provides feedback to the control circuit.



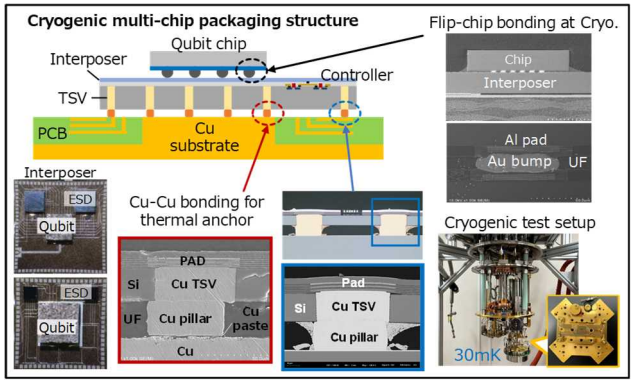
2. Outcome so far

We have developed a cryogenic quantum control circuit, including 16-bit bias voltage generators, for controlling silicon qubits from the 4K stage of a dilution refrigerator. To achieve further precise control, we also developed a cryogenic analog-to-digital converter (Cryo-ADC) that enables signal acquisition and qubit readout in the 100 mK temperature, which is closer to the qubits. For this ADC, a new circuit architecture was designed to simultaneously meet stringent power constraints and achieve wideband performance. A prototype chip based on this design was fabricated, and it was confirmed to operate correctly at 100 mK with a power consumption of 30 uW. Furthermore, the Cryo-ADC was applied to the quantum environmental monitoring system. By employing an equivalent sampling technique, we successfully achieved pulse signal acquisition with 1ns time resolution in close to the qubits.



As part of the development of cryogenic multi-chip packaging technology, an advanced chip implementation structure was developed to integrate qubit and interface chips.

In addition, chip-level thermal management techniques were explored to enable efficient dissipation of heat generated during qubit operation. A cryogenic packaging was developed in which through-silicon vias (TSVs) were formed in a silicon interposer, enabling both signal transmission and heat dissipation. To construct a high-thermal-conductivity path, Cu pillars were formed on the TSVs and bonded to a Cu substrate via Cu-Cu bonding. Thermal cycling tests were conducted using a cryogenic refrigerator to evaluate the reliability. We confirmed the connectivity remained through the cross-sectional view even after the tests. Currently, we prepare the evaluation for thermal dissipation characteristics of this structure by employing the temperature monitoring technique.



3. Future plans

We will implement cryogenic quantum control circuits and environmental monitoring system in actual qubit experiments to evaluate their impact on control fidelity. In addition, we will verify the effectiveness of TSV signal transmission and heat dissipation experimentally. These activities contribute to the development of circuit and packaging platforms for large-scale silicon quantum computers.

R&D Item

3. Hot silicon qubits

Progress until FY2024

1. Outline of the project

In this Item, we aim to achieve "high-temperature" operation of silicon qubits, referred to as “hot silicon qubits” (Fig. 1). This involves operating the qubits around 1 Kelvin (K), equivalent to around -272 degrees Celsius. This is higher than the typical operating temperature of solid-state qubits, which is a few tens of millikelvin (mK). By achieving hot silicon qubits, we can improve the permissible circuit power consumption (heat dissipation) and enable closer placement of cryogenic control circuitry. This contributes to the development of large-scale integrated silicon quantum computers. To achieve high-performance hot silicon qubits, we are exploring the "sweet spot" where quantum coherence time is maximized and comparing electron spin and hole spin systems.

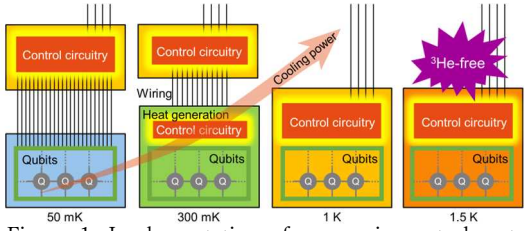


Figure 1: Implementation of cryogenic control systems through high-temperature operation of qubits.

2. Outcome so far

Development of elemental techniques for the realization of hot silicon qubits.

① Manipulation: As a 2024 milestone, we observed the coherent time evolution of hole spins at ~1K. In addition, we are advancing technical developments to achieve high-fidelity operation at higher temperatures. For the first time, we demonstrated extension effect of spin phase relaxation time (T_2^{Rabi}) using phase-modulated microwaves on hole spins (Figure 2).

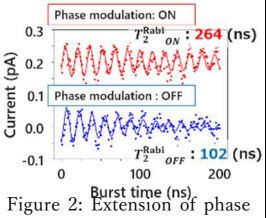


Figure 2: Extension of phase relaxation time by phase modulated microwaves

② Readout: Radio-frequency (RF) reflectometry measurement method, which is considered promising for high-temperature readout, is a technique used to read the state of a qubit by analyzing the reflectivity of RF signals applied to the qubit system. We achieved the evaluation of spin relaxation time(T_1), the length of time that quantum information can be stored in a qubit, using the technique we developed (Figure 3). [C. Kondo, et al, Jpn. J. Appl. Phys. 64, 01SP09 (2025)]

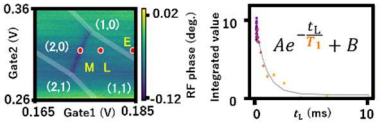


Figure 3: Spin relaxation time evaluation

③ Efforts toward scalability: We are conducting research aimed at scalability from multiple approaches. To realize integrated qubit structures, we proposed a two-dimensional array structure that allows for high-speed and individual control despite its high-density configuration. Additionally, we developed an automatic quantum dot tuning technique using model-based reinforcement learning, which minimizes time-consuming learning processes, unlike other methods. [C. Kondo, et al., APL Mach. Learn. 3, 016114 (2025)] We also evaluated the temperature dependence of charge noise and found that in the hole spin system, noise levels do not significantly increase with temperature rises to 1K, suggesting its promise for high-temperature operation. Furthermore, we are advancing the development of integration techniques for qubits and their control with cryogenic classical circuits. Through collaboration with Kobe University, we confirmed the expected characteristics at 4K for a silicon qubit chip flip-mounted on an interposer. [T. Futaya et al., Jpn. J. Appl. Phys. 63, 03SP64 (2024)] Additionally, we demonstrated selective control using selector circuits implemented on the same interposer.

④Outreach activities: The realization of silicon quantum computers requires the development and integration of individual elemental technologies and techniques. Therefore, it is important to disseminate these technologies to researchers across various fields. For this purpose, we summarized and presented the research trends and prospects of semiconductor qubits, as well as individual elemental technologies and challenges. [T. Kodera, JSAP Rev. 2024, 240101 (2024), etc.] We are also committed to nurturing future quantum human resources who will lead future research and development. We cooperated in holding events such as the QIH-MS6 Co-hosted Quantum Technology Spring School.

3. Future plans

We will evaluate and verify the operation of silicon qubits at 1K by utilizing the knowledge of issues related to higher temperatures and fidelity improvement and techniques for initialization, readout, and manipulation of qubits that we have accumulated up to this fiscal year. In addition, we will conduct benchmark test of electron spin and hole spin systems.

R&D Item

4. Quantum computing in small qubit systems

Progress until FY2024

1. Outline of the project

The project aims to identify early-stage challenges in developing a silicon-based large-scale quantum computer by utilizing small-scale experimental circuits as foundational elements for future large-scale silicon qubit array structures.
As shown in Fig. 1, we are using experimental circuits equipped with well-established qubit operations to evaluate and improve fundamental processes such as qubit initialization, readout, and coherent control. By integrating these functions, we demonstrate quantum operations and assess the feasibility of fault-tolerant quantum computation in large systems. Furthermore, this research provides design guidelines for scalable qubit array structures and contributes to the overall project goals.

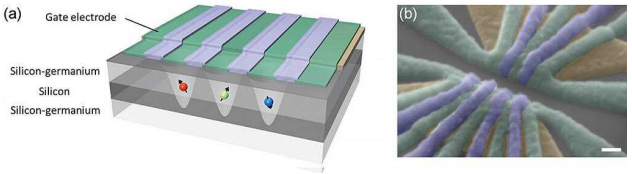


Fig. 1 Schematic of a Si/SiGe device hosting fully controllable three spin qubits (left) and its scanning electron micrograph image (right). The scale bar indicates 100 nm (one ten-millionth of a meter).

2. Outcome so far

Our outcomes can be categorized into the following six key areas:
1. Methods for initialization and readout in qubit arrays
2. Universal control of three spin qubit
3. High-fidelity two-qubit gate operations for fault tolerance
4. Balancing qubit control speed and operational errors
5. Phase-flip error correction code with three spin qubits
6. Assessment of qubit error correlations

Point 1 involves establishing methods for initializing and reading out qubits within a one-dimensional silicon qubit array——a process that had been previously challenging.

In Point 2, we demonstrated universal quantum control over three silicon qubits and, for the first time, successfully synthesized a tripartite entangled state with a high fidelity of 88%.

Points 3 and 4 involve achieving high-fidelity controlled-NOT operations between two qubits, overcoming a major bottleneck in this system. A gate fidelity of 99.5% was demonstrated, meeting the threshold for fault-tolerant operations. We derived guidelines for further fidelity improvement by optimizing speed-noise trade-offs.

In Point 5, we integrated high-fidelity control of three qubits to realize the world's first phase-flip error correction circuit using silicon qubits (Fig. 2), making a major milestone toward fault-tolerant silicon quantum computers.

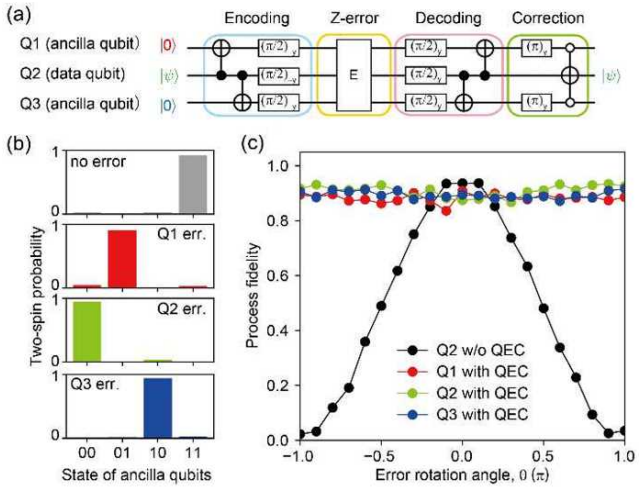


Fig. 2 Phase-flip error correction experiment using three spin qubits in silicon. (a) Quantum circuit. (b), (c) Results.

In Point 6, we analyzed error correlations between adjacent qubits, which poses a challenge in quantum error correction within array structures. Measurements of phase precession rate fluctuations that cause errors in silicon qubits (Fig. 3) revealed strong local correlations that decay with distance. Additionally, we developed methods to characterize noise sources based on these correlations, including a new technique for evaluating charge noise correlations in qubit devices. These findings will contribute to the future design and performance improvement of silicon quantum computers.

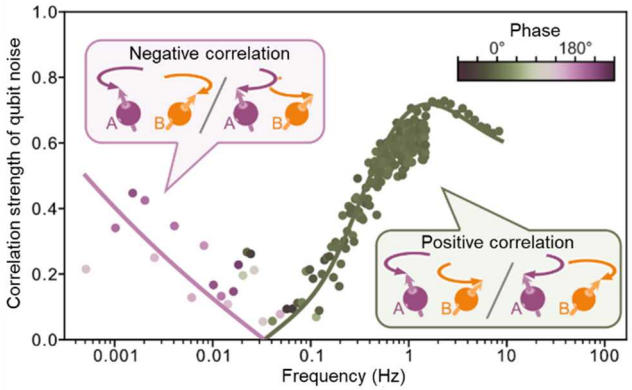


Fig. 3 Correlation spectrum of qubit phase fluctuations.

3. Future plans

To realize fault-tolerant quantum computers, we will continue developing strategies to scale up qubit systems without compromising performance. A deeper understanding of error correlations in silicon qubits will guide this effort. We aim to establish scalable control methods—including initialization, readout, and operation—while taking into account the specific characteristics and constraints of silicon qubits and array structures, with an eye toward applications in large-scale system.