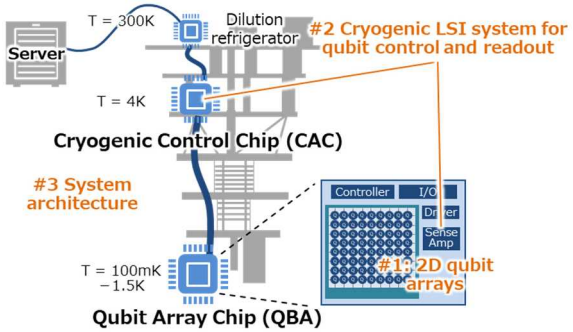
R&D Theme

Quantum Computing System

Progress until FY2022

1. Outline of the project

This theme is responsible for overseeing the entire project and organizing the quantum computer as a system, and is working on three specific R&D challenges (#1, #2, and #3).

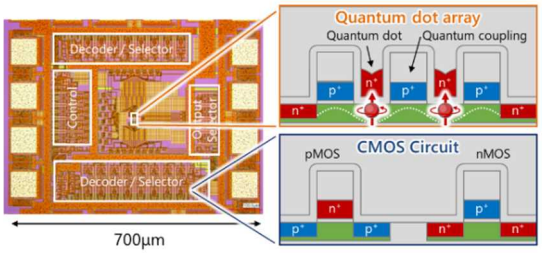


The first is research on the "2D qubit array" of qubits, which is a milestone of large-scale silicon quantum computers. The second is the development of "Cryogenic LSI system for qubit control and readout." which are necessary to control the large-scale qubit array. Third, we are developing the "system architecture" to operate the system as a computer. Through these efforts, we aim to realize a large-scale silicon quantum computing system that takes full advantages of the features of silicon semiconductor technology.

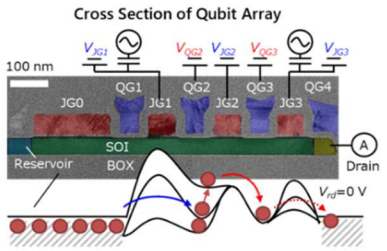
2. Outcome so far

(1) Develop embedded-qubit CMOS process (QCMOS)
(2) Develop new schemes for initialization, readout, and operation for the qubit arrays
(3) Investigate the possibility of qubit operation in the array
(4) Prototype of cryogenic qubit control chips
(5) Develop of quantum operating systems

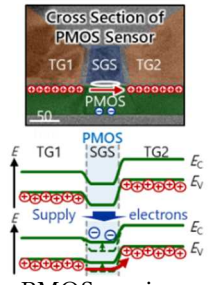
As an example, in (1), we developed and evaluated a 65-nm QCMOS process for qubit array chip (QBA), which enables 2D qubit arrays to be embedded in a CMOS chip with small modification of the process. [N. Lee et al., SSDM2021]



In (2), we developed a single-electron pumping technique that stores electrons one at a time in the quantum dots for qubit initialization, and confirmed high accuracy and stable operation. [T. Utsugi et al., JJAP2023] As an alternative to the widely-used low-density RF reflectometry, we have developed and evaluated a small-size PMOS sensing technique with nA-order sensitivity that can be integrated peripherally to the array. [D. Hisamoto et al., APEX2023]

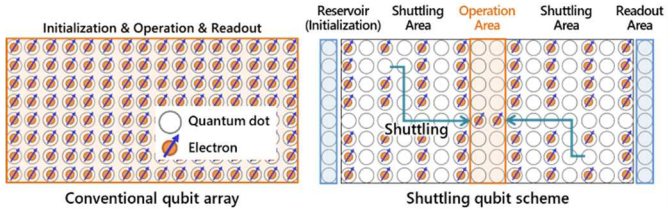


Single-electron pumping

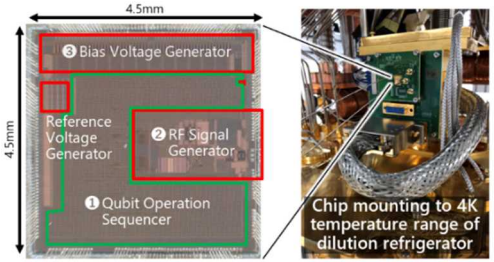


PMOS sensing

Furthermore, regarding qubit operation, we have proposed "Shuttling qubit method," which achieves qubit operation and readout by moving (shuttling) the electrons within the array, whereas conventionally the electrons that form a qubit are fixed at the location of the quantum dots in which they are stored. [Hitachi News Release (6/12/2023)]



In (4), we have fabricated a 40-nm CMOS cryogenic control chip (CAC) that generates more than 50 channels of bias signals and low-jitter RF signals for qubit array control. We are currently evaluating the chip by implementing it in the 4K temperature region of a dilution refrigerator.



3. Future plans

Many innovations are essential to reach the goal. Collaboration within and outside the project will enable qubit operation in a qubit array structure, and furthermore, system-level implementation will improve the reliability and efficiency of the qubit operations.

国立研究開発法人 科学技術振興機構 Japan Science and Technology Agency

Here begins our new MIRAI
MOONSHOT RESEARCH & DEVELOPMENT PROGRAM

R&D Theme

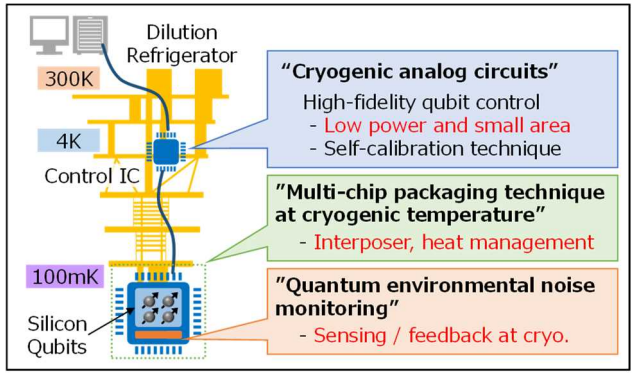
Multi-chip cryogenic packaging technology

Progress until FY2022

1. Outline of the project

The main R&D theme of this project is to develop cryogenic circuit and implementation techniques for large-scale silicon quantum computers. This enables high-fidelity control and high-density implementation of a large number of silicon qubits, thereby contributing to the realization of error-tolerant quantum computers for Moonshot Goal 6.

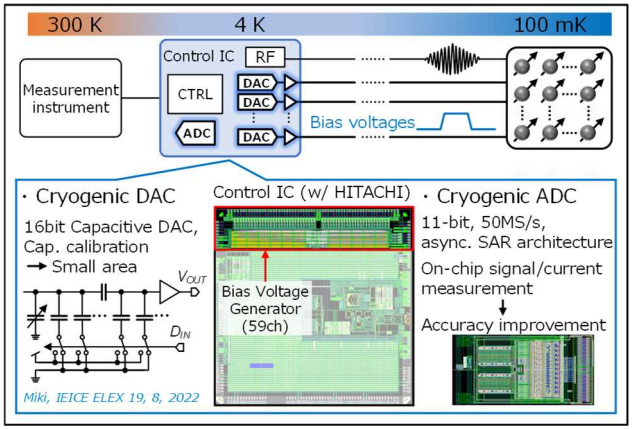
In order to achieve this, we are tackling the following three challenging themes. First, we are developing ultra-small, low-power cryogenic analog circuits which enable control of numerous qubits inside a dilution refrigerator. Second, we are creating innovative packaging by integrating qubit chips and their interface functionality on an interposer to accommodate large-scale qubits within the refrigerator. Furthermore, we are establishing a monitoring technique that observes quantum environmental noise affecting the accuracy of qubits and provides feedback to the control circuit.



2. Outcome so far

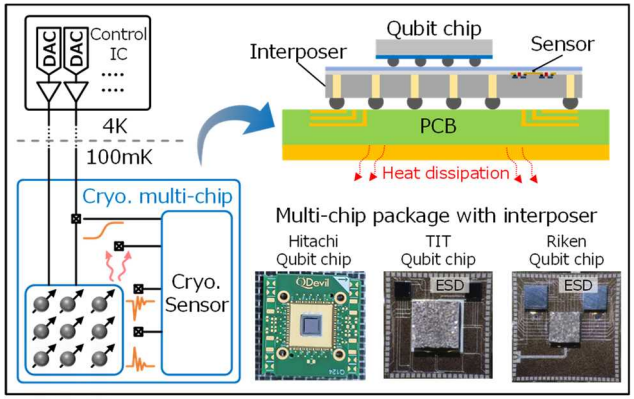
①Design of cryogenic DA/AD converters for qubit control
②Development of multi-chip packages for stacking qubit chips
③Implementation of environmental sensor near the qubits

In the above outcome①, we developed an IC chip to control silicon qubits from the 4K stage of a dilution refrigerator. Specifically, we worked on the design of a 16-bit cryogenic DAC that generates the bias voltages for qubits, and a cryogenic ADC which measures each control signal inside the chip. The cryogenic DAC is required to be small area since a large number of channels are installed for controlling 64 qubits. Therefore, we invented novel architecture which effectively utilizes cryogenic characteristics and calibration technique for mismatch, integrating a 59-channel voltage generator into a single chip. Furthermore, we completed performance evaluations at 4K and confirmed that it operates correctly.



In ②, we developed silicon interposers for flip-chip mounting of the silicon qubit chips. We have constructed a multi-chip package by stacking qubit chips from HITACHI, Tokyo Institute of Technology and RIKEN, which are part of the same project, and we are currently measuring the qubit characteristics. In addition, we are developing a manufacturing process which achieves efficient signal routing and heat dissipation by forming through-silicon vias in the silicon interposers.

In ③, we designed cryogenic sensor circuit to acquire quantum environmental noise that affects the control precision of qubits, such as the temperature, power supply noise and control signal waveform near the qubits. This sensor circuit is placed at the 100 mK stage, thus we proposed a new sensor architecture that can operate with only 1 μW. We mounted this sensor on the interposer developed in ②, and confirmed that it properly operates at room temperature.



3. Future plans

We will experiment qubit control using the cryogenic control IC. Moreover, we continue qubit experiments with the multi-chips in which qubit chips are stacked, and develop feedback method for information acquired by monitoring sensor, to contribute on the realization of large-scale silicon quantum computers.

国立研究開発法人 科学技術振興機構 Japan Science and Technology Agency

R&D Theme

Hot silicon qubits

Progress until FY2022

1. Outline of the project

In this theme, we aim to achieve "high-temperature" operation of silicon qubits, referred to as “hot silicon qubits” (Fig. 1). This involves operating the qubits around 1 Kelvin (K), equivalent to around -272 degrees Celsius. This is higher than the typical operating temperature of solid-state qubits, which is a few tens of millikelvin (mK). By achieving hot silicon qubits, we can improve the permissible circuit power consumption (heat dissipation) and enable closer placement of cryogenic control circuitry. This contributes to the development of large-scale integrated silicon quantum computers. To achieve high-performance hot silicon qubits, we are exploring the "sweet spot" where quantum coherence time is maximized and comparing electron spin and hole spin systems.

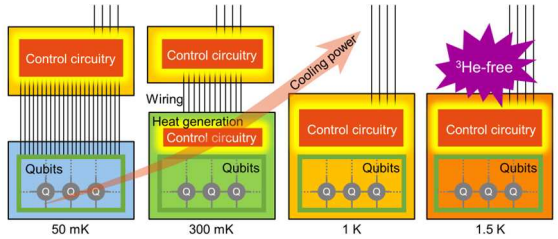


Figure 1: Implementation of cryogenic control systems through high-temperature operation of qubits.

2. Outcome so far

① We verify the required characteristics for qubit operation in the developed silicon qubit structures.

② We overview the current status and challenges of essential technologies for silicon quantum computers.

③ We confirm that the increase in noise associated with temperature rise is suppressed in the hole spin system.

①: We tested a part of silicon qubit array for qubit operations (Fig. 2). The qubit device showed the expected change in an energy level with magnetic fields, which will allow us to control its spin operation frequency. We also successfully detected single-electron tunneling events in real-time towards reading the spin state. These advancements bring us closer to realizing silicon qubits.

② : We summarized the current status and challenges in a silicon quantum computing. The summary includes discussions on the “quality” (indivisual qubit performance) and the “quantity” (approaches for large-scale integration). It is published to support researchers from various fields in the development of silicon quantum computers.

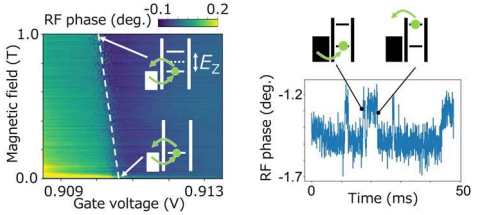


Figure 2: (left) Magnetic field dependence of an electron spin energy. (right) Real-time detection of single electron tunneling events.

③ : We investigated the temperature dependence of charge noise in the hole spin system (Fig. 3). The results reveal low noise levels up to 1 K, demonstrating promising performance at higher temperatures. Additionally, at 300 mK, the noise level was comparable to previous studies on electron spins in quantum dots measured at 50 mK or lower.

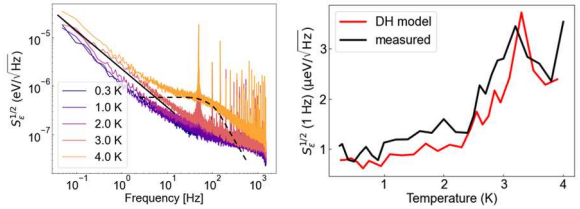


Figure 3: Noise increase with higher temperatures. (left) Noise spectrum density. (right) Noise magnitude at 1 Hz.

3. Future plans

Based on our accumulated knowledge on improving fidelity, our current focus is on demonstrating qubit operation. We aim to demonstrate the operation of silicon qubits at relatively high temperatures, such as 300 mK and even 1 K. This involves performing qubit initialization and readout under appropriate control voltage conditions and utilizing alternating magnetic or electric fields for state control.

R&D Theme

Quantum computing in small qubit systems

Progress until FY2022

1. Outline of the project

The project aims to demonstrate quantum algorithms using a small number of high-fidelity spin qubits in silicon. We unveil technical challenges in quantum operations and control techniques, which are expected to be crucial in future large-scale silicon quantum computers.

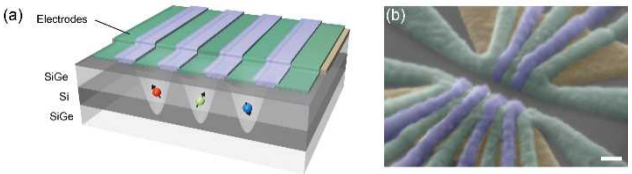


Fig.1 (left) Schematic of 3-qubit device. (right) Scanning electron micrograph. Scale bar, 100 nm (1 nm = 10^{-9} m).

We implement quantum algorithms in Si/SiGe quantum dot devices where high-fidelity control of spin qubits has been established (Fig.1). We explore the feasibility of fault-tolerant quantum computation that requires high-fidelity initialization, readout, and coherent control.

2. Outcome so far

①Measurement and initialization of qubits in the middle of quantum dot arrays.

②Universal quantum control of three spin qubits

③High-fidelity two-qubit gate for fault tolerance

④Mitigation of control errors in high-speed manipulations

⑤Phase-flip error correction with three spin qubits

In ①, we have implemented initialization and readout of a spin qubit in the middle of a quantum dot array using SWAP operations. This technique allows us to scale up the system to a longer array where many qubits are not directly accessible from reservoirs.

We have then demonstrated universal control of three spin qubits in ②. We have generated a three-spin entangled state (GHZ state) with a fidelity of 88%.

We have also investigated high-fidelity two-qubit control in ③ and ④. By optimizing the speed of quantum gates and the effect of noise, we have realized a controlled-NOT gate with a fidelity as high as 99.5% which is believed to be sufficient for fault-tolerant quantum computation (Fig.2).

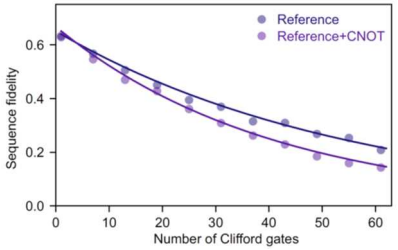


Fig.2 Characterization of CNOT gate fidelity by randomized benchmarking.

Finally, we have demonstrated quantum error correction using a three-qubit phase-flip code in ⑤. This is a big step toward fault-tolerance silicon quantum computers.

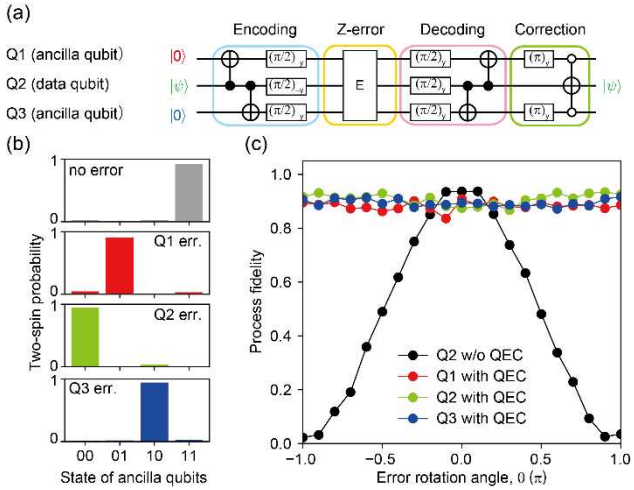


Fig.3 Quantum error correction with a Si 3-qubit device.

3. Future plans

Practical quantum error correction requires fast, high-fidelity qubit readout in addition to high-fidelity control. Since the readout of silicon spin qubits is orders of magnitude slower than control, we plan to improve it using the RF reflectometry technique and the Pauli spin blockade phenomenon. We further explore the feasibility of larger arrays of silicon spin qubits by connecting distant qubits via electron shuttling.