

3. Development of isotopically controlled Si/SiGe substrate technology

Progress until FY2024

1. Outline of the project

The R&D Item aims to develop isotopically controlled silicon-silicon germanium (Si/SiGe) substrate materials required to mount qubit devices and medium-range quantum couplings for the realization of fault-tolerant silicon quantum computers. A high-quality quantum-well substrate with isotope Si-28 embedded in a SiGe thin-film is required to maximize the performance of qubits and freely array qubits.

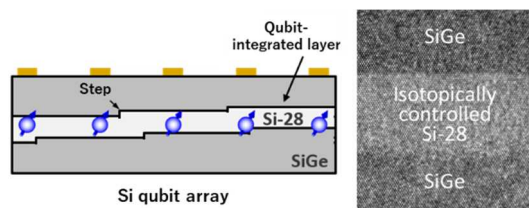


Fig. 1 Schematic of isotopically controlled Si/SiGe substrate with an integrated qubit array (left) and cross-sectional electron micrograph (right).

In this Item, we will work on the development of (1) isotope control technology that is capable of depositing high-quality isotope layers, (2) fundamental technology for interface control that suppresses atomic steps at the hetero-interface, and (3) process technology to extensively evaluate the material performance of isotope substrates. Eventually, we will try to build a new quantum technology to realize a large-scale fault-tolerant Si quantum computer while maintaining compatibility with the semiconductor industry.

2. Outcome so far

(1) Development of isotope control technology that enables high-quality film deposition

To ensure reliable operation of a qubit array and coherent transfer of qubit states over middle-range distances, it is important to achieve high-quality isotope substrates on the scale of qubit integration and to ensure uniformity of potentials within the isotope structure. We have developed prototypes of isotope substrates with reduced impurity concentrations that act as charge traps, improved interface steepness and flatness in the isotope layer, and suppressed inhomogeneity caused by distortion and compositional fluctuations.

(2) Development of fundamental technology for interface control using light elements

As a method for suppressing the generation of interfacial steps based on an understanding of the microscopic origin of interfacial steps that can interfere with qubit arrays, we focused on the reciprocal properties of a light element, such as defect termination and bond breaking, and devised a new interface control technique by modifying the internal structure of the isotope substrate. We have developed a technique to precisely measure the structural factor representing the step spacing of the isotope interface. Based on this technique, we are currently conducting tests to verify efficient localized hydrogen introduction and its suppression of interfacial tilting.

(3) Development of large-area process evaluation technology for isotope substrates

We have been working on the development of technology to evaluate device performance over a wide range of defects inherent in isotope substrates. We have designed and fabricated a device with a one-dimensional split-gate type array for measurement of charge noise in isotope substrates. In addition, we implemented a certain number

of Si/SiGe qubits in the isotope substrate with enhanced interface flatness developed in (1), and investigated the performance, including the valley-splitting property necessary for improving qubit controllability. We found that this leads to giant valley separation and its non-uniformity depending on the position of neighboring qubits. Thus we obtained the knowledge necessary to extract the intrinsic performance of isotope substrates and scale-up policy that satisfy the fault-tolerance requirement.

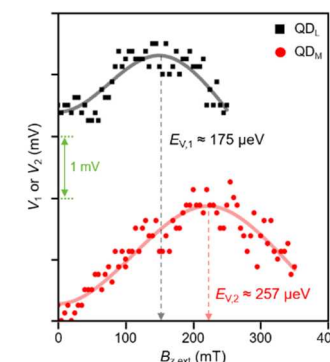


Fig. 2 Valley characteristics of Si/SiGe qubits mounted on isotopically controlled substrates

3. Future plans

We will advance the technological development of high-grade, scalable isotopically controlled Si/SiGe substrates that can implement the large-scale qubit arrays. In parallel, we will work to verify the principle of interface control technology by introducing light elements and to improve the practicality of isotope substrates. In the future, we will aim to establish a new scaling technology that links the quality of isotope substrates and the device performance of qubits for a fault-tolerant silicon quantum platform.