R&D Item

5. Frontend Analog RF LSI at Room Temperature

Progress until FY2024

1. Outline

Currently, in a qubit controller operating at room temperature, a front-end analog RF part (Fig. 1) for transmitting and receiving microwave control signals consists of compound semiconductor devices, bipolar devices, and numerous discrete components with excellent high-frequency and low-noise characteristics, resulting in a large mounting size and high-power consumption. To increase the number of qubits in the future, it is necessary to drastically reduce the mounting size and power consumption of the front-end analog RF part. In this project, PLL (Phase Locked Loop), transmitter (TX), and receiver (RX), which are essential functional blocks in the front-end analog RF part, have been developed utilizing advanced CMOS process technologies to ensure proper operation at room temperature, with the goal of miniaturization and low power consumption. In addition, the improvement of isolation between transmitter and receiver, which is a challenge in integration, was examined.

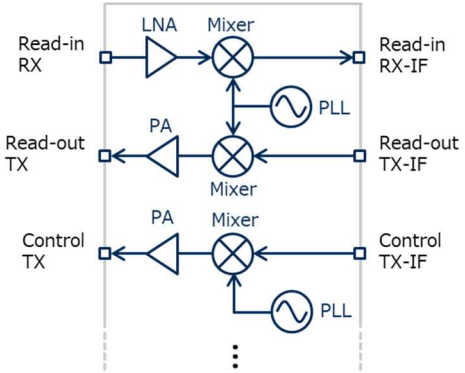
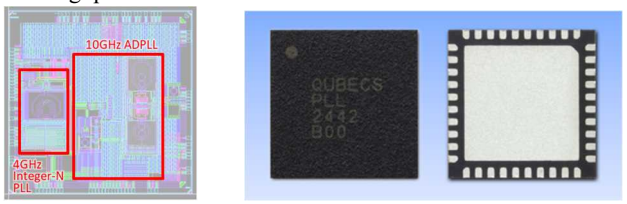


Fig. 1. Example block diagram of Qubit front-end analog RF part (partially illustrated)

2. Outcome so far

As an effort to reduce power consumption and noise in the PLL, the PLL comparison frequency was set to 1 GHz and the PLL band was widened to reduce PLL in-band noise. The signal frequency of 1 GHz was generated by a simple Integer-N PLL. In addition, All Digital PLL (ADPLL) operating at a comparative frequency of 1 GHz by utilizing the fine CMOS process technologies has been designed.

The performances of the fabricated PLL prototype test chip (Fig. 2) were evaluated. The measured PLL in-band phase noise at the output frequency of 10 GHz was -105dBc/Hz, which is similar performance of the PLL installed in an existing qubit controller. In addition, for long-term phase fluctuation, which is important for qubit controllers, 0.12 ° rms was confirmed for the ADPLL alone in a measurement system based on a rubidium oscillator with a measurement time of 1,000 seconds and a measurement time resolution of 40 milliseconds. The power consumption of the developed PLL was about 80% lower than that of the PLL in the existing qubit controller.

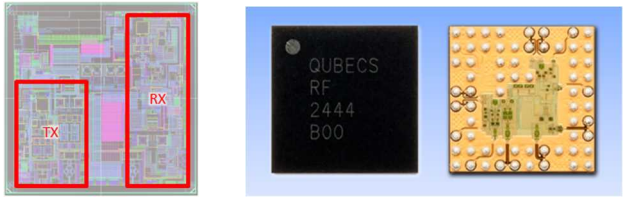


(a) Chip layout (b) Package

Fig. 2. PLL prototype test chip

To reduce the reviver noise, a 10 GHz-band CMOS low-noise amplifier (LNA) has been developed based on an inductively degenerate common-source topology effective for noise cancellation. The transistors used in the LNA were designed using several layout techniques that minimize parasitic components to reduce signal loss at high frequencies. To improve signal leakage from transmitter to receiver, a power amplifier (PA) uses a clover-type transformer for the load to suppress magnetic leakage. Furthermore, a fully differential circuit configuration with well-matched pair layouts was adopted for the LNA and the PA to suppress the signal leakage. To verify the effectiveness of our approach, a test chip containing both a transmitter and a receiver was fabricated utilizing 22nm Silicon On Insulator (SOI) process (Fig. 3). The die was packaged in a Fan Out Wafer Level Package (FOWLP), which exhibits excellent high-frequency characteristics. The test chip mounted on the PCB was measured at room temperature.

The 10 GHz-band CMOS LNA achieved a noise figure (NF) of approximately 2.5 dB, confirming the industry-leading NF as a CMOS LNA with ESD (Electro-Static Discharge) protection. The NF characteristics of the developed LNA showed relatively good agreement with the simulation results. In addition, the PA achieved an output power of more than 10 dBm at 10 GHz, which is equivalent to that of the existing qubit controller, despite the low voltage operation. Furthermore, a target isolation of 70 dB or more between transmission and reception is achieved while integrating the transmitter and receiver on the same die. The power consumption of the transmitter and receiver was approximately 1/10 of that of the existing qubit controller.



(a) Chip layout (b) Package

Fig. 3. Transmitter and Receiver prototype test chip

3. Future plans

After completing the performance evaluation of the test chip, a design guideline for CMOS integration will be proposed based on the evaluation results and identified issues.