R&D Item

# 4. Front-end and Back-end Cryo CMOS

## Progress until FY2024

### 1. Outline

We will develop ASICs (application-specific integrated circuits) and SoCs (system-on-chips) that can operate stably in cryo (cryogenic 4K) with the goal of developing devices for building scalable systems. We have developed a prototype SoC (System on a Chip) integrating four circuit blocks: digital circuit (Sine Wave Generator) in Task 1, PLL (Phase-Locked Loop) in Task 2, DAC in Task 3, and ADC in Task 4, and confirmed its normal operation at cryo (Figure 1 ). However, there is a problem with the performance of the DAC at cryo, and a new prototype is scheduled for development in 2025.

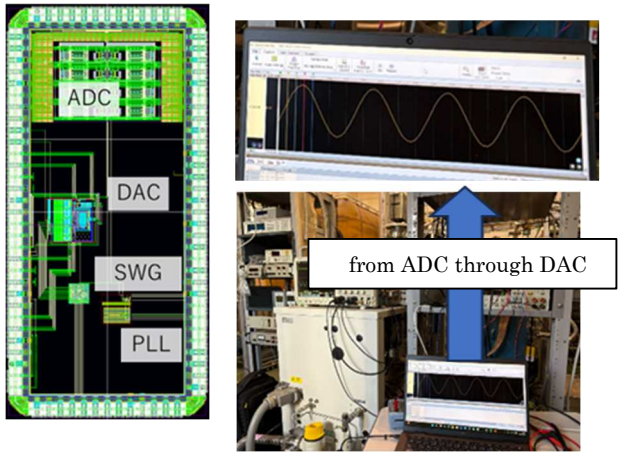



Figure 1 : Prototype SoC layout and measurement results at cryo temperature (4.2K)

### 2. Outcome so far

In the Items 1, 4, and 5, the digital signal processor (DSP) RTL was modified for ASIC from an FPGA implementation. This 22 nm bulk process ASIC is now in its second design iteration, incorporating SRAM macros operating at 4K and converting some operations to floating point with smaller bit widths.

In the Item 2, we continued device modeling and design evaluation for RF front-end circuits in cryo. Our wiring resistance model was confirmed and improved through measurements, leading to a practical model (Figure 2). We also designed a PLL clock generation, confirming its 4K operation. RF signal source and mixer circuits were designed using the 22nm CMOS process.

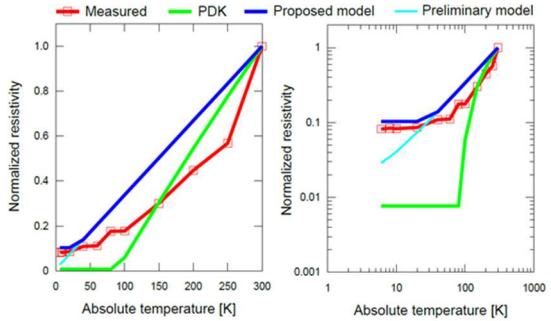
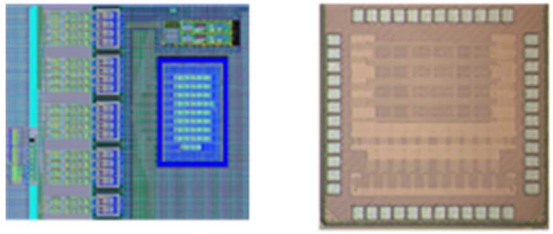



Figure 2 : Resistance of various types of wiring as temperature

In the Item 3, we involved measuring a 12-bit, 2 Gsps DAC designed in the 22 nm CMOS process at room temperature and 4 K. Due to poor linearity, the effective number of bits (ENOB) was 6 bits, falling short of expectations. However, we established a 4K measurement environment and identified improvement areas for future prototypes. Additionally, Bayesian optimization achieved automatic design of an 8-bit unitary DAC in under 6 hours, with future work focusing on scaling to 12 bits.

In the Item 4, we designed an 8-channel time-interleaved ADC (Figure 3a) using a 22-nm bulk CMOS process for high-speed cryo operation. A mismatch correction circuit for time-interleaved operation was also designed, and test chips (Figure 3b) were fabricated. The ADCs operated normally at room temperature and in liquid helium (4.2K), successfully developing a 10-bit resolution, 2 Gsps sampling rate ADC.



(a) 12-bit DAC layout (b) 8ch ADC chip

Figure 3 : Image of prototype chip

### 3. Future plans

In the next fiscal year, a prototype of an improved SoC integrating a digital circuit, DAC, ADC, and RF-PLL will be developed. The prototype SoC will be measured not only at KEK but also at a cryostat to be installed at Kyoto Institute of Technology. Design and prototyping of elemental circuits for digital, ADC, DAC, and RF sections for 2025 and beyond will also be conducted. In the digital circuit, a prototype GCDRAM memory array will be built and its operation as a macro will be verified.