R&D Item

1. Error Correction Algorithm for Hardware and Backend System with FPGA

Progress until FY2024

1. Outline

This R&D Item is to develop an error correction backend system that can perform error syndrome analysis required for error correction at high speed and low latency. To this end, the following three tasks are being implemented. Task 1 is to develop error correction hardware for fast, low latency, and scalable error syndrome analysis, and an error correction backend (BE) system using FPGA cluster. In Task 2, to investigate the performance improvement of the BE system by optimizing the hardware implementation method, we study the ASIC implementation of the main part of the quantum error correction (QEC) core circuit and evaluate its performance. In Task 3, we develop a high-performance and reliable interconnection network technology between the quantum front-end (FE) developed in Item 2 and our BE, as well as a reliable FPGA cluster technology to prepare for larger-scale BE.

2. Outcome so far

1. Error Correction Hardware and FPGA Clusters

We developed and optimized a syndrome subgraph algorithm for efficient execution on FPGA hardware, further extending it for parallel processing across multiple FPGAs. Evaluations using a custom software simulator confirmed that algorithm optimization and parallelization significantly improved the logical error rate. We implemented this algorithm as a QEC circuit module on an FPGA using AFU Shell, verifying its functionality and assessing its resource consumption and operating frequency relative to code distance. For multi-FPGA parallelization, our primary approach involves distributing the output of the reduction unit to numerous final matching units across many FPGAs.

2. Evaluation of QEC Cores for ASICs

We investigated specific hardware implementation and optimization methods for ASIC-based QEC cores. By synthesizing logic and performing placement and routing, we quantitatively assessed the performance of each elemental circuit to identify ASIC implementation bottlenecks. A central component, the error decoder, was evaluated using a test chip, leading to the development of a superior ASIC micro-architecture. Measurements from test chips fabricated with a 22-nm CMOS process confirmed its advantages over previous decoders. Simulation also validated the performance improvements of our proposed ASIC optimization.

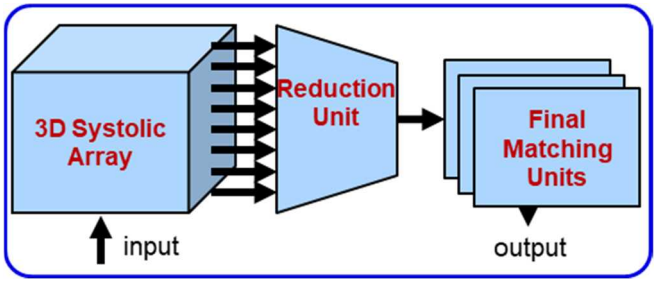

Fig. 1. Hardware design of the syndrome subgraph algorithm with multiple final matching units.

3. Realization of a Dependable Error Correction Backend For the FE-BE demonstration system

We developed an FPGA-implemented method to reduce network bandwidth by merging Ethernet frames carrying syndrome information from the front end (FE). To facilitate development without a physical FE, we deployed a front-end emulator that streams pre-generated syndrome data at actual rates. This emulator can simulate network traffic from up to 36 FEs, adequate for current physical qubit counts. Additionally, to enhance communication efficiency within the BE's FPGA cluster, we explored a high-speed, low-latency, many-to-many communication scheme as an Ethernet alternative and developed proof-of-concept hardware.

3. Future plans

To realize an error correction backend system that can handle scalable processing with multiple FPGAs, we have been developing the basic technical elements of the system, such as quantum error correction algorithm, its hardware design, FPGA SoC, and a network between front end (FE) and back end (BE). In the future, we plan to implement a BE system of parallel quantum error correction hardware with an FPGA cluster while continuing to improve the algorithm and demonstrating its scalability for quantum error correction on the scale of 100 physical qubits. Furthermore, in collaboration with Item 2, we plan to construct a demonstration system connecting FE and BE to demonstrate quantum error correction using actual superconducting quantum devices or quantum error simulation results.