Development of Integration Technologies for Superconducting Quantum Circuits

R&D Theme Name

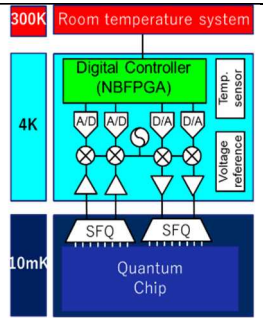
Research and development of electronics for quantum error correction

Progress by FY2022

1. Overview

In the typical setup of today's superconducting qubit circuits, a qubit chip placed at cryogenic temperatures and microwave electronics operating at room temperature is wired together by one or more coaxial cables per qubit. However, due to limitations in space and cooling capacity of the refrigerator, this method cannot handle the scale-up of qubits. To solve this problem, this R&D theme aims to develop qubit control and readout electronics that operate as close to the qubit as possible and to break through the wiring bottleneck for integration. In this development, the challenge is how to realize a control system that efficiently performs quantum error correction within the limited space and cooling capacity of a refrigerator.

This R&D theme focuses on single flux quantum circuits, which can operate at several tens of GHz and have ultra-low power consumption, and atomic-switched FPGAs, which are highly flexible, capable of advanced processing, and have low power consumption, to develop low-temperature electronics systems in which they work together.

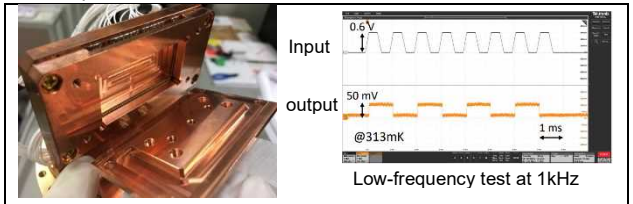


Low-temperature electronics for qubit control and readout

2. Results by FY2022

① Successful operation of a single flux quantum circuit using a low critical current density process

Single flux quantum (SFQ) circuits have been designed primarily for operation at 4 K. However, this research and development requires operation at 10 mK, which is the same as that of a qubit, and requires further reduction in power consumption of conventional SFQ circuits. Therefore, we are designing devices and fabricating chip prototypes with the aim of "reducing the critical current values of the Josephson junctions of the SFQ circuits to 1/10 or less," which is necessary for ultra-low power consumption. Last year, we tested the operation of a signal transmission circuit with the reduced power consumption of 1/50 at liquid helium temperature (4.2 K) on a prototype chip and obtained the expected signal at low speed. At lower temperatures, changes in device characteristics must also be considered. This year, we prepared an evaluation environment at 0.3 K and confirmed circuit operation at that temperature.

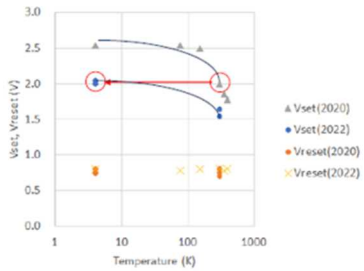


Low-frequency test at 1kHz

Waveforms of SFQ circuit operated at 0.3K

② Confirmation of rewrite operation at 4 K for a stand-alone nanobridge

We are developing FPGAs that can operate at low temperatures to support a variety of correction algorithms for error correction processing. FPGAs are designed to operate at 4 K. This research project is centered on developing an atom switch (NanoBridge) FPGA that can operate at low temperatures, which consumes 1/4 the power at room temperature compared to commercially available CMOS-based FPGAs. By last fiscal year, we had fabricated a prototype NanoBridge using a standard CMOS process (65 nm) and confirmed its programming at 4K. This fiscal year, we succeeded in reducing the programming at 4K to the same level as that at room temperature by improving the manufacturing process. We also completed the circuit design of a NanoBridge FPGA for 4K operation using a process design kit for low-temperature, which was developed last fiscal year.



Reduced programming voltage of NanoBridge at 4K

3 Future Developments

For SFQ circuits, we will build a design library using various parameters extracted at cryogenic temperatures through prototype evaluation and proceed to design circuits such as qubit control signal demultiplexers. For nanobridges, based on the established design guidelines, we will specifically begin manufacturing NanoBridge FPGAs and fabricate chips.

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