Here begins our new MIRAI
MOONSHOT RESEARCH & DEVELOPMENT PROGRAM

R&D Theme

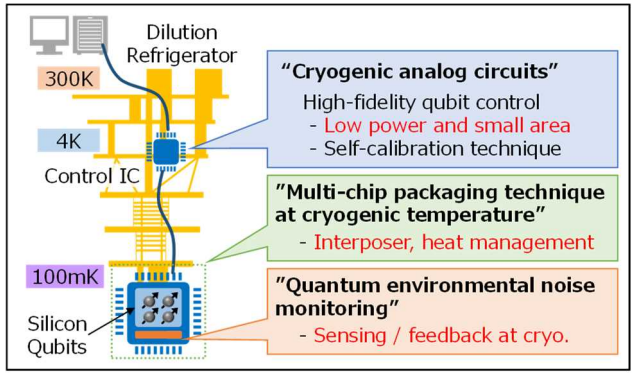
Multi-chip cryogenic packaging technology

Progress until FY2022

1. Outline of the project

The main R&D theme of this project is to develop cryogenic circuit and implementation techniques for large-scale silicon quantum computers. This enables high-fidelity control and high-density implementation of a large number of silicon qubits, thereby contributing to the realization of error-tolerant quantum computers for Moonshot Goal 6.

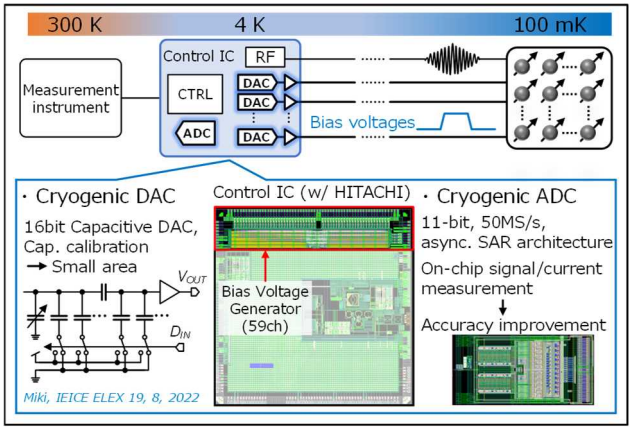
In order to achieve this, we are tackling the following three challenging themes. First, we are developing ultra-small, low-power cryogenic analog circuits which enable control of numerous qubits inside a dilution refrigerator. Second, we are creating innovative packaging by integrating qubit chips and their interface functionality on an interposer to accommodate large-scale qubits within the refrigerator. Furthermore, we are establishing a monitoring technique that observes quantum environmental noise affecting the accuracy of qubits and provides feedback to the control circuit.



2. Outcome so far

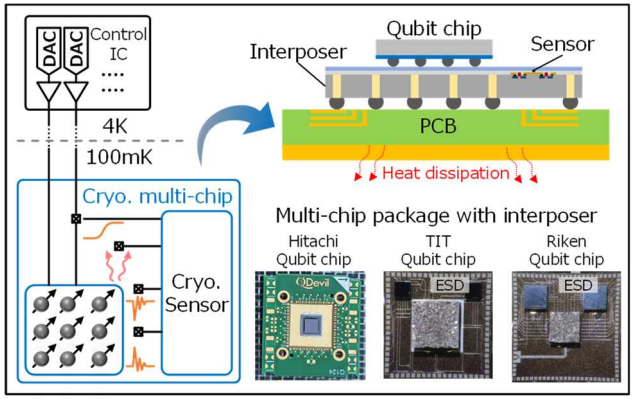
①Design of cryogenic DA/AD converters for qubit control
②Development of multi-chip packages for stacking qubit chips
③Implementation of environmental sensor near the qubits

In the above outcome①, we developed an IC chip to control silicon qubits from the 4K stage of a dilution refrigerator. Specifically, we worked on the design of a 16-bit cryogenic DAC that generates the bias voltages for qubits, and a cryogenic ADC which measures each control signal inside the chip. The cryogenic DAC is required to be small area since a large number of channels are installed for controlling 64 qubits. Therefore, we invented novel architecture which effectively utilizes cryogenic characteristics and calibration technique for mismatch, integrating a 59-channel voltage generator into a single chip. Furthermore, we completed performance evaluations at 4K and confirmed that it operates correctly.



In ②, we developed silicon interposers for flip-chip mounting of the silicon qubit chips. We have constructed a multi-chip package by stacking qubit chips from HITACHI, Tokyo Institute of Technology and RIKEN, which are part of the same project, and we are currently measuring the qubit characteristics. In addition, we are developing a manufacturing process which achieves efficient signal routing and heat dissipation by forming through-silicon vias in the silicon interposers.

In ③, we designed cryogenic sensor circuit to acquire quantum environmental noise that affects the control precision of qubits, such as the temperature, power supply noise and control signal waveform near the qubits. This sensor circuit is placed at the 100 mK stage, thus we proposed a new sensor architecture that can operate with only 1 μW. We mounted this sensor on the interposer developed in ②, and confirmed that it properly operates at room temperature.



3. Future plans

We will experiment qubit control using the cryogenic control IC. Moreover, we continue qubit experiments with the multi-chips in which qubit chips are stacked, and develop feedback method for information acquired by monitoring sensor, to contribute on the realization of large-scale silicon quantum computers.

国立研究開発法人 科学技術振興機構 Japan Science and Technology Agency