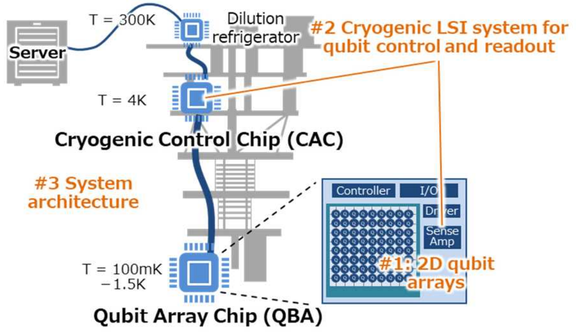
R&D Theme

Quantum Computing System

Progress until FY2022

1. Outline of the project

This theme is responsible for overseeing the entire project and organizing the quantum computer as a system, and is working on three specific R&D challenges (#1, #2, and #3).

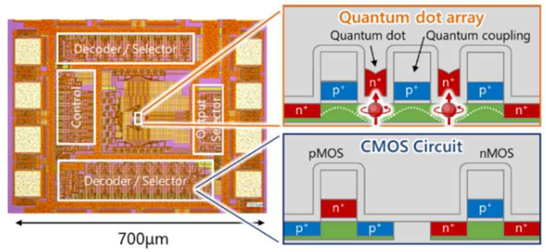


The first is research on the "2D qubit array" of qubits, which is a milestone of large-scale silicon quantum computers. The second is the development of "Cryogenic LSI system for qubit control and readout." which are necessary to control the large-scale qubit array. Third, we are developing the "system architecture" to operate the system as a computer. Through these efforts, we aim to realize a large-scale silicon quantum computing system that takes full advantages of the features of silicon semiconductor technology.

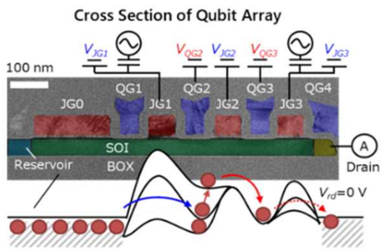
2. Outcome so far

(1) Develop embedded-qubit CMOS process (QCMOS)
(2) Develop new schemes for initialization, readout, and operation for the qubit arrays
(3) Investigate the possibility of qubit operation in the array
(4) Prototype of cryogenic qubit control chips
(5) Develop of quantum operating systems

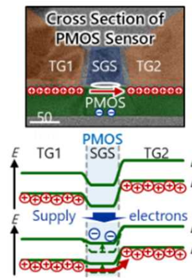
As an example, in (1), we developed and evaluated a 65-nm QCMOS process for qubit array chip (QBA), which enables 2D qubit arrays to be embedded in a CMOS chip with small modification of the process. [N. Lee et al., SSDM2021]



In (2), we developed a single-electron pumping technique that stores electrons one at a time in the quantum dots for qubit initialization, and confirmed high accuracy and stable operation. [T. Utsugi et al., JJAP2023] As an alternative to the widely-used low-density RF reflectometry, we have developed and evaluated a small-size PMOS sensing technique with nA-order sensitivity that can be integrated peripherally to the array. [D. Hisamoto et al., APEX2023]

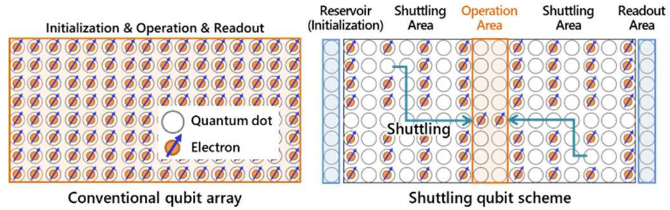


Single-electron pumping

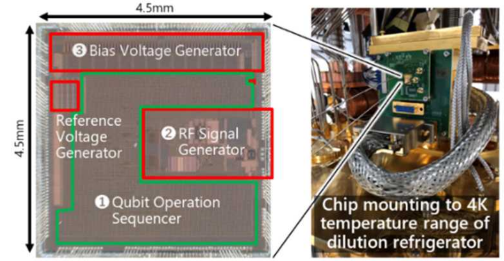


PMOS sensing

Furthermore, regarding qubit operation, we have proposed "Shuttling qubit method," which achieves qubit operation and readout by moving (shuttling) the electrons within the array, whereas conventionally the electrons that form a qubit are fixed at the location of the quantum dots in which they are stored. [Hitachi News Release (6/12/2023)]



In (4), we have fabricated a 40-nm CMOS cryogenic control chip (CAC) that generates more than 50 channels of bias signals and low-jitter RF signals for qubit array control. We are currently evaluating the chip by implementing it in the 4K temperature region of a dilution refrigerator.



3. Future plans

Many innovations are essential to reach the goal. Collaboration within and outside the project will enable qubit operation in a qubit array structure, and furthermore, system-level implementation will improve the reliability and efficiency of the qubit operations.