R&D Theme

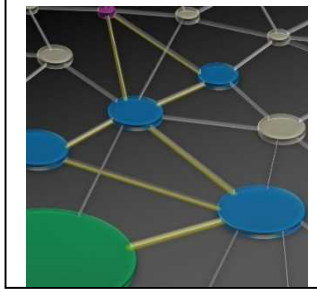
Research and development of distributed fault-tolerant quantum computers

Progress until FY2022

1. Outline of the project

Under this theme, we aim to explore the possibility of distributed architecture of fault-tolerant quantum computers. In particular, the goal is to open up the possibilities of quantum computation with physical systems that cannot be scaled up without having a distributed structure and of further scaling up by connecting quantum computers that are developed in a monolithic form. This will present new guidelines for the design of fault-tolerant quantum computers, eventually contributing to the realization of a fault-tolerant quantum computer in 2050, i.e., the goal of the Moonshot Goal 6.

Toward the goal, we have started to consider the design of a basic module to connect distant qubits or integrated chips with quantum communication, as well as the exploration of quantum error-correcting codes and fault-tolerant quantum computing schemes which fit distributed architecture.

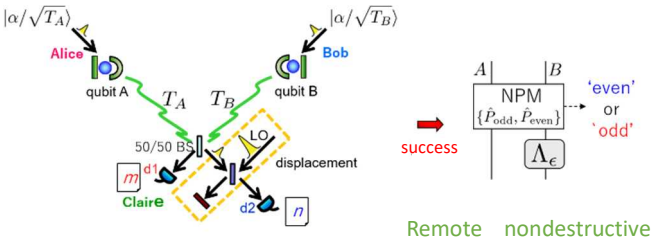


Distributed fault-tolerant quantum computer

2. Outcome so far

1) Optimal supplier of single-error type entanglement via coherent-state transmission [K. Azuma *et al.*, PRA **105**, 062432 (2022)]

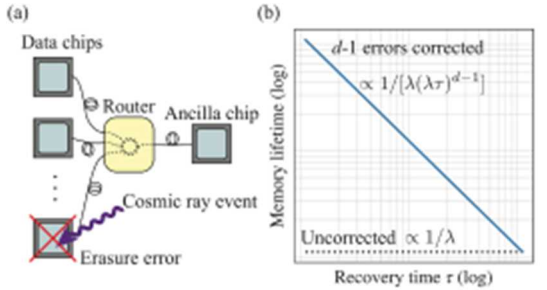
The basis of distributed quantum computation is to apply a high-fidelity controlled-not gate to distant qubits, which is achieved by supplying them with high-fidelity entanglement. In this research, we derive an upper bound on achievable rates of protocols that supply single-error type entanglement via coherent-state transmission over lossy channels. This upper bound coincides with the performance of an existing protocol based on a remote nondestructive parity measurement. Our result suggests that if we perform distributed quantum computing based on such an efficient entanglement distribution protocol, entanglement distillation may not be necessary in terms of performance, in contrast to what was thought to be required in existing proposals.



Remote nondestructive parity measurement

2) Distributed quantum error correction for chip-level catastrophic errors [Q. Xu *et al.*, PRL **129**, 240502 (2022)]

It has been pointed out that a large-scale quantum computer may suffer from cosmic ray events that cause chip-level catastrophic errors. We proposed to implement quantum error correction across separate chips in a distributed quantum-computing setup. Even if arbitrary data in a chip is destroyed, by connecting data chips and an ancilla chip, the data as a whole can be retrieved with an erasure quantum error correcting code. Our scheme can, for example, suppress the rate of such catastrophic errors from 1 per 10 s to less than 1 per month.



(a) Proposed scheme; (b) Recovery time vs memory lifetime

3. Future plans

We will develop a blueprint of a distributed fault-tolerant quantum computer, by building a found practical basic module into distributed architecture of quantum computing.

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