Moonshot International Symposium for Goal 6

2021/04/23

"Research and Development of
Theory and Software for Fault-tolerant Quantum Computers"

Masato Koashi (Project Manager)

The University of Tokyo

Projects in Moonshot Goal 6

MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

Integration Technologies for Superconducting Quantum Circuits

Quantum Computing with Photonically Interconnected Ion Traps

Large-scale Fault-tolerant Universal Optical Quantum Computers

Large-scale Silicon Quantum Computer

Quantum Interfaces for Building Quantum Computer Networks

Quantum Cyberspace with Networked Quantum Computer

Theory and Software

Layers in fault-tolerant universal quantum computer

Applications

Tasks given to the quantum computer

Compiling with pre/post processing

Decomposition into given instruction sets with optimizations

Logical qubits and error correction

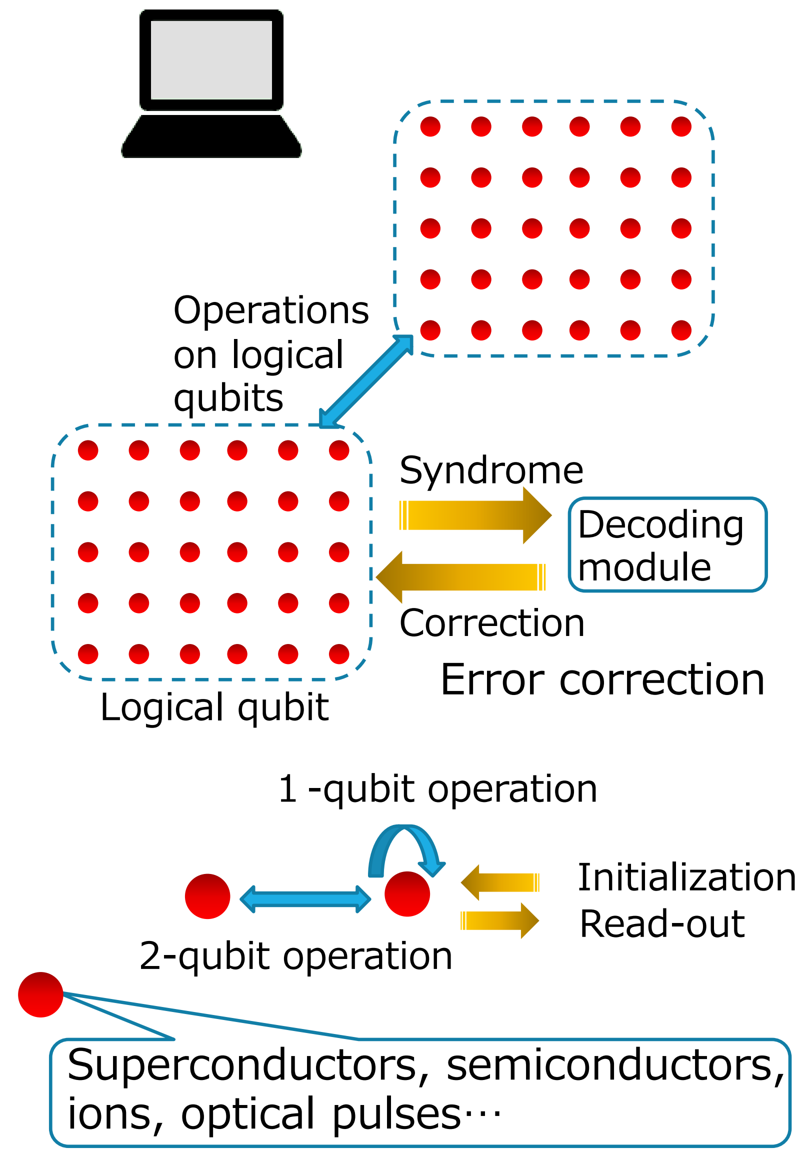
Quantum error correcting codes
Fault-tolerant error correction schemes
Logical instruction sets

Controlling Qubits

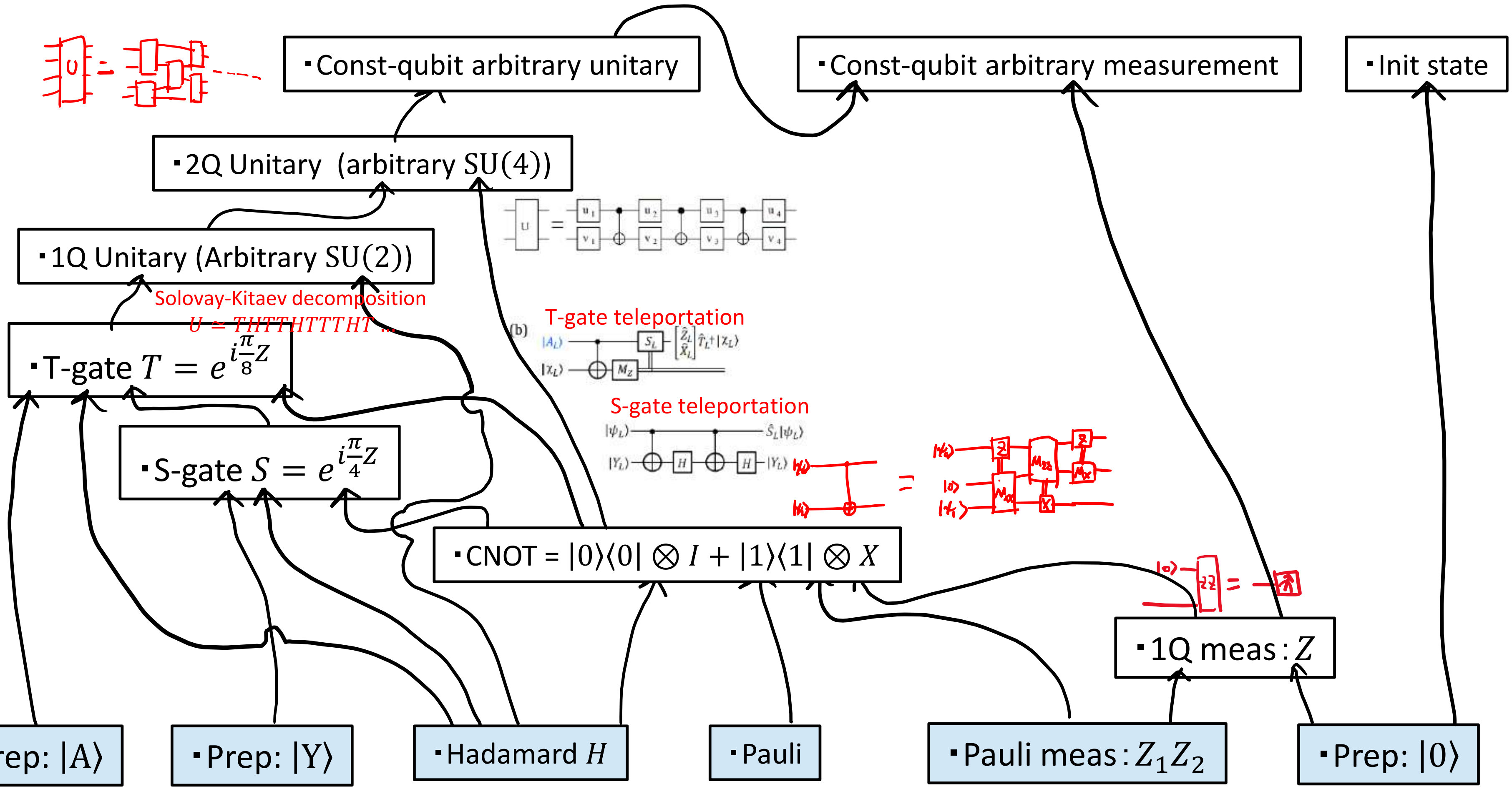
Initialization, gate operations, read-out

Designing Qubits

Physical qubits using various hardware (lifetime, interaction, scalability ...)



Logical instruction set (example)



Layers in fault-tolerant universal quantum computer

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Logical qubits and error correction

Logical instruction set

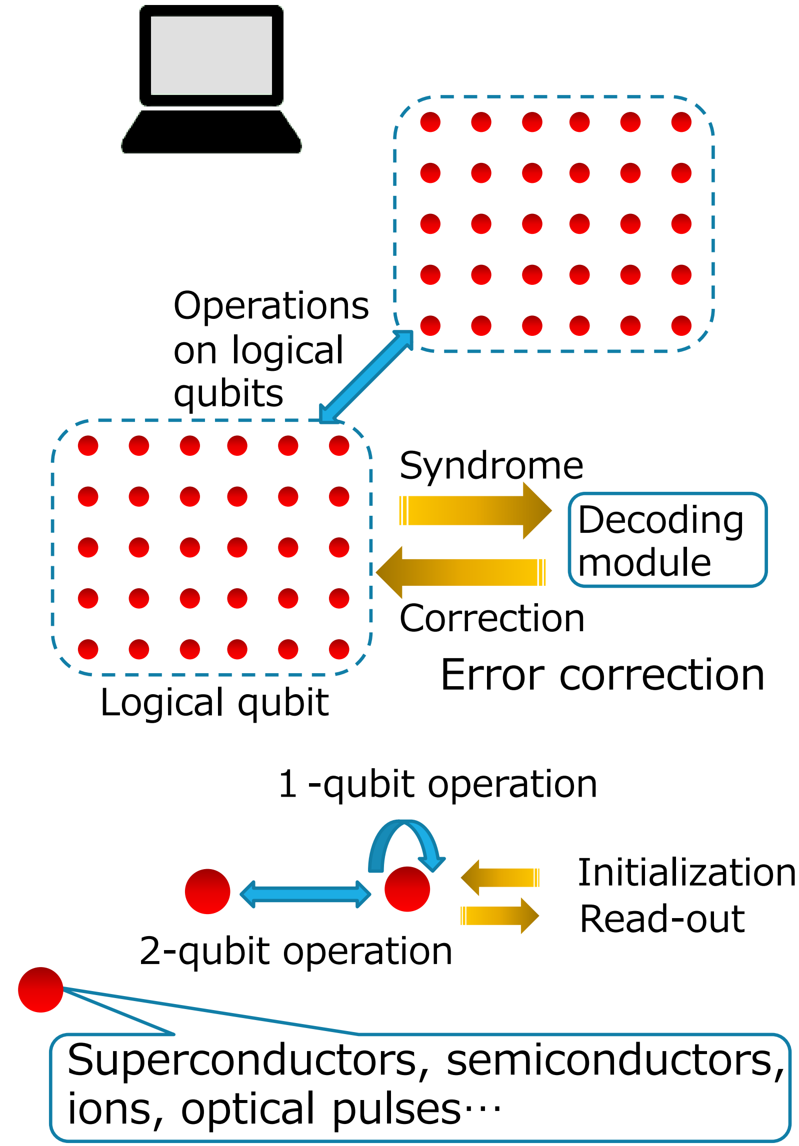
- Prep: $|A\rangle$
- Prep: $|Y\rangle$
- Hadamard H
- Pauli
- Pauli meas : $Z_1 Z_2$
- Prep: $|0\rangle$

es

out

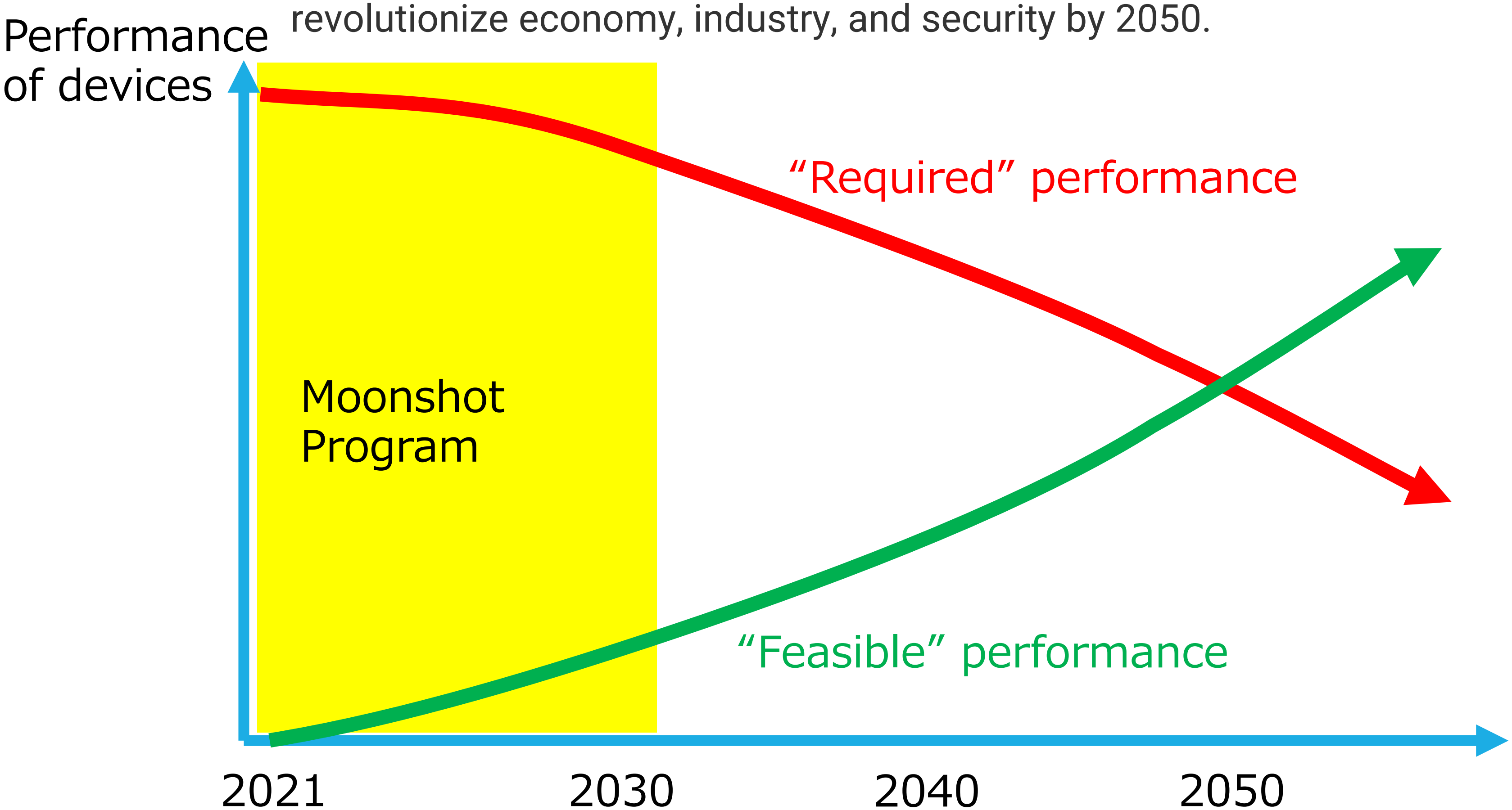
Designing Qubits

Physical qubits using various hardware (lifetime, interaction, scalability ...)



Mission for Theory/Software PJ

Moonshot Goal 6:
Realization of a fault-tolerant universal quantum computer that will revolutionize economy, industry, and security by 2050.



Mission for Theory/Software PJ

Substantially reducing the device performances required for large-scale fault-tolerant quantum computer.

Layers in fault-tolerant universal quantum computer

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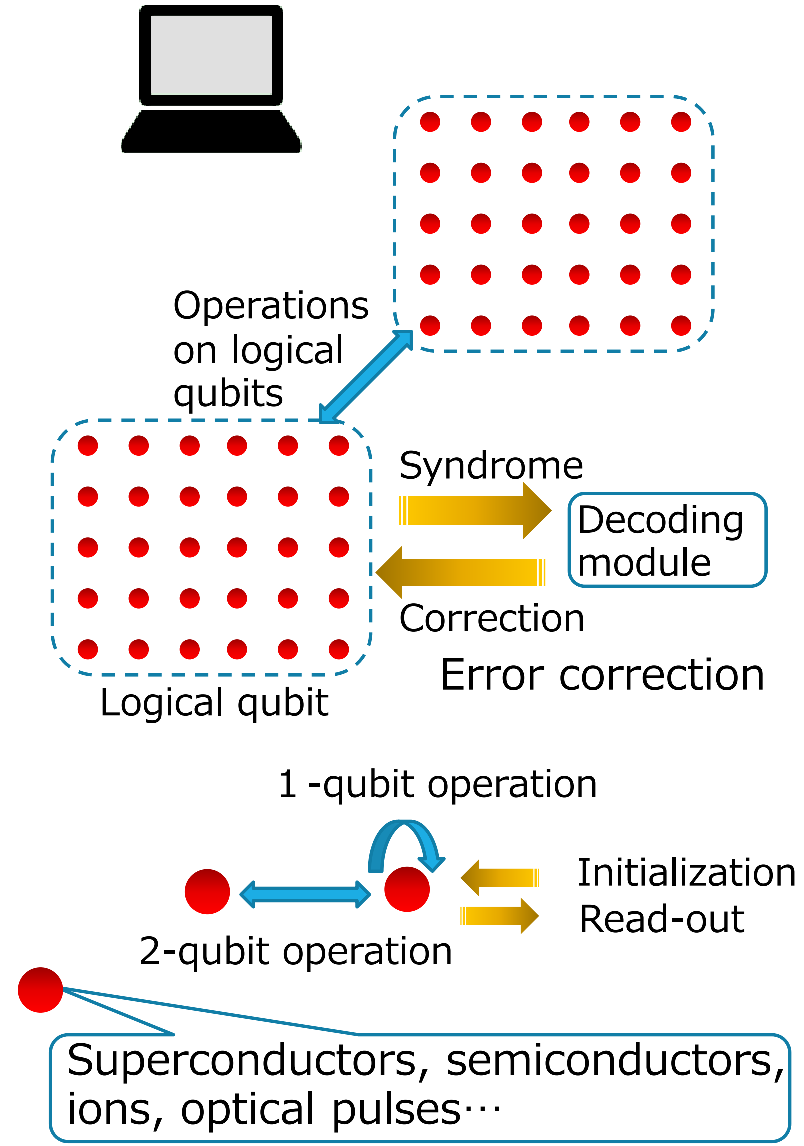

Projects in Moonshot Goal 6

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Theory and Software

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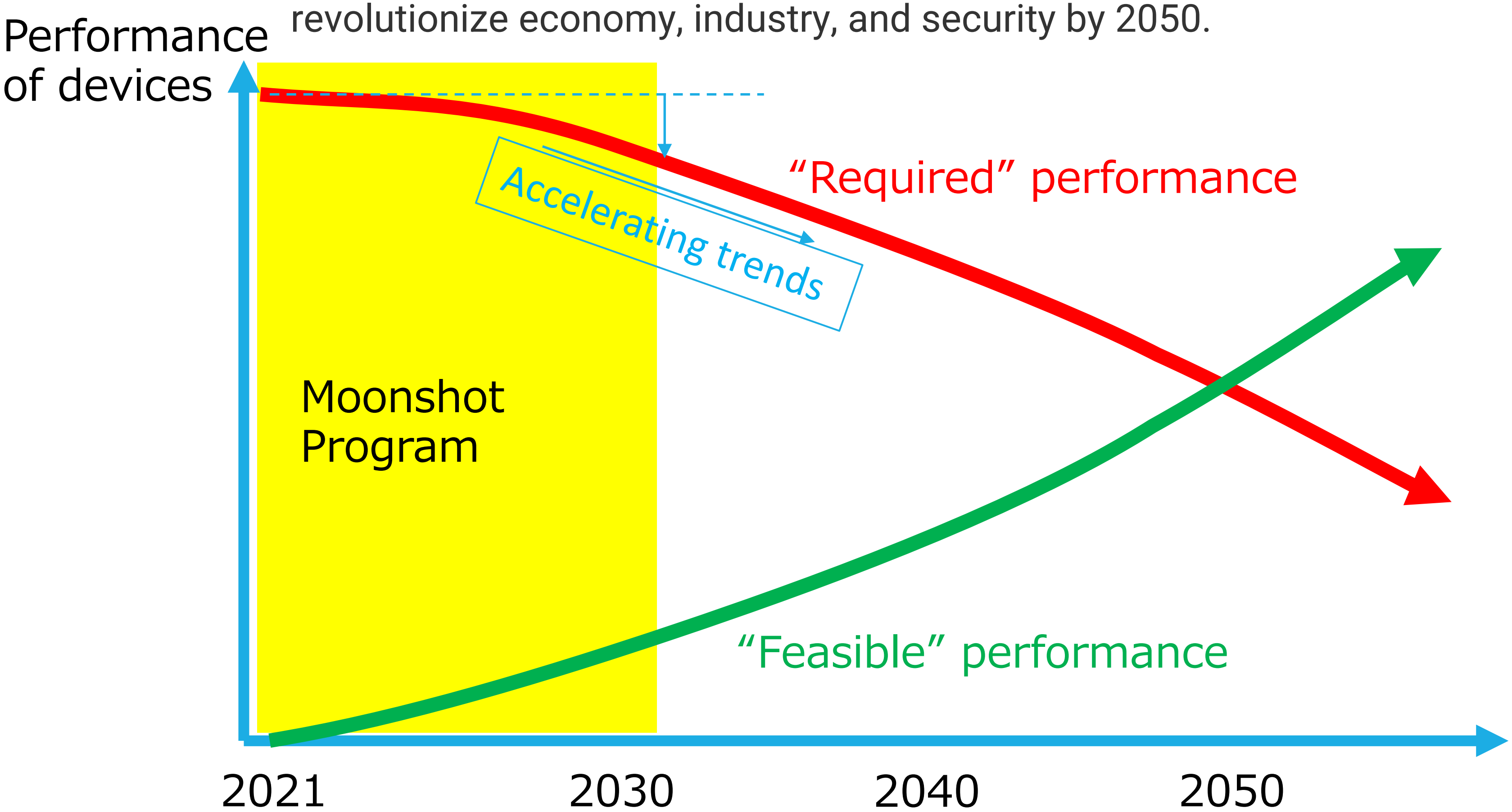


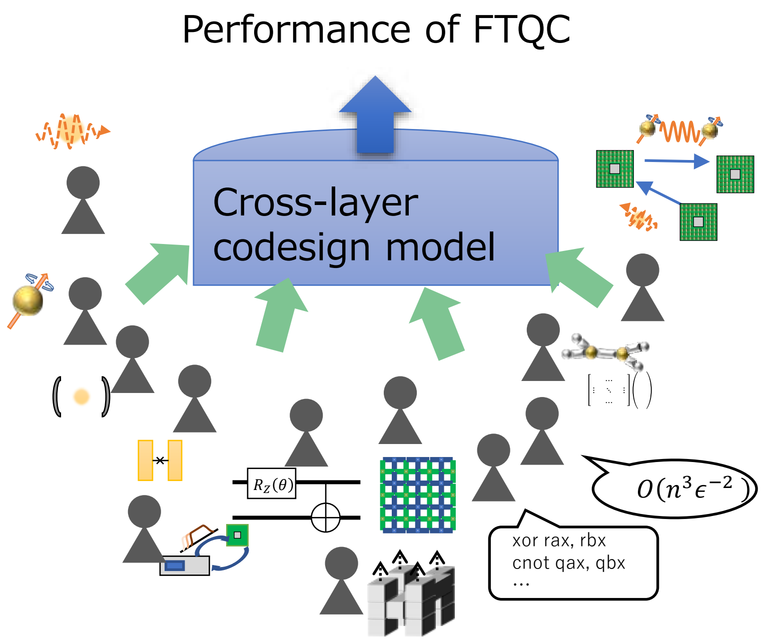
Mission for Theory/Software PJ

Substantially reducing the device performances required for large-scale fault-tolerant quantum computer.

Cross-layer co-design model

・A fault-tolerant universal quantum computer (FTQC) is a complicated system with many layers, such as designing qubits, controlling qubits, error correction, compiling, applications.

・A cross-layer codesign model encompasses metrics and trade-off relations in these layers, and through optimizations and simulations, predicts the performance of the FTQC.



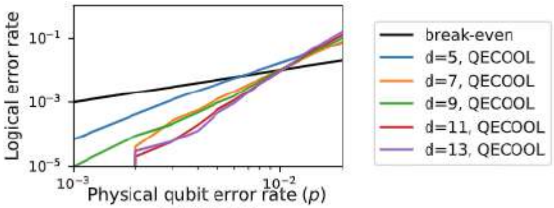
Case in point:

On-line decoder with SFQ-based superconducting digital circuits.

Required clock cycles

	$p = 0.001$			$p = 0.005$			$p = 0.01$		
d	Max	Avg	σ	Max	Avg	σ	Max	Avg	σ
5	104	6.10	4.99	144	10.4	11.2	166	15.6	15.8
7	303	11.8	14.5	515	28.7	30.1	557	47.4	43.9
9	800	22.7	30.6	1018	64.2	57.7	1308	107	89.7
11	996	41.6	53.6	1779	120	95.3	2435	201	161
13	1890	71.3	82.9	3289	199	147	4072	337	266

Logical error rates



(c) 2 GHz

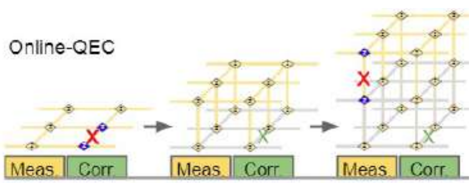
Code distance d Physical qubit error rate p

External constraints

Cooling capacity
Fabrication technology

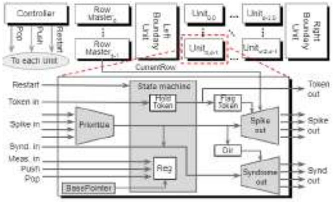
Design error correction cycles

design of parity check pipeline

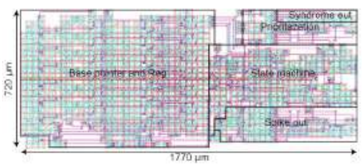


Design decoding logics

State machines



Chip implementation



Y. Ueno, M. Kondo, M. Tanaka, Y. Suzuki, Y. Tabuchi, arXiv:2103.14209, to appear in Proc. IEEE/ACM Design Automation Conference (DAC) 2021.

Case in point:

Parameters passed to compilers

Logical instruction latency

Logical instruction error rate

Required clock cycles

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d	Max	Avg	σ	Max	Avg	σ	Max	Avg	σ
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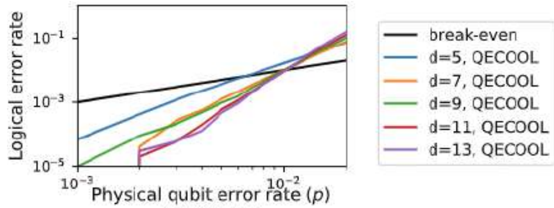
Logical error rates



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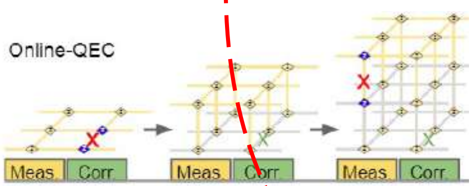

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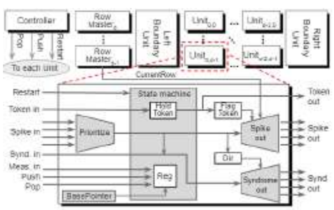

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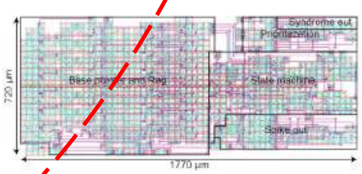

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Parameters in physical layers

Qubit lifetime

Physical gate time & error rate

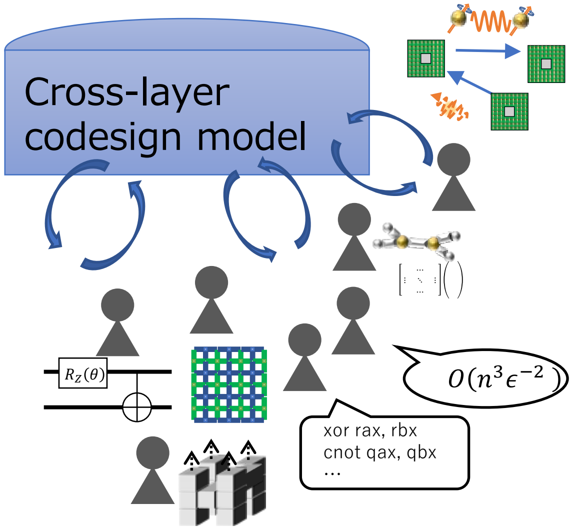
Cross-layer codesign model

・In the development stage of the cross-layer codesign model, it works as a hub to promote research in the Theory/Software Project.

Encouraging interactions among them

Letting them communicate in the same language

Helping them see the big picture toward the Goal of the Moonshot program.



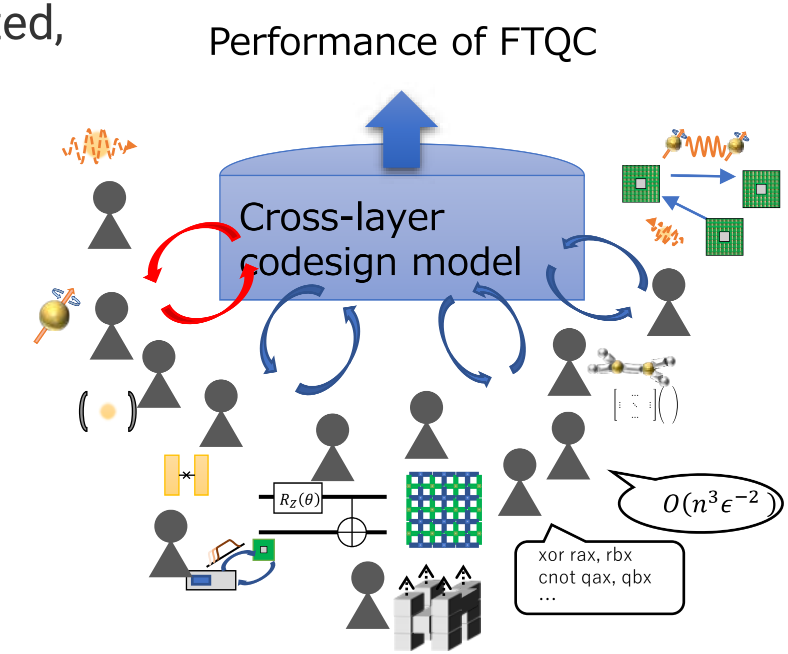
Cross-layer codesign model

・In the development stage of the cross-layer codesign model, it works as a hub to promote research in the Theory/Software Project.

・Once the prototype of the model is constructed, it will work as a pilot to guide the researchers (theoretical/experimental) in the Moonshot Program toward its Goal.

Trade-offs in various levels:
Choice of parameters in hardware design
Allocation of time and money

Hard to know what is the best within a single layer.



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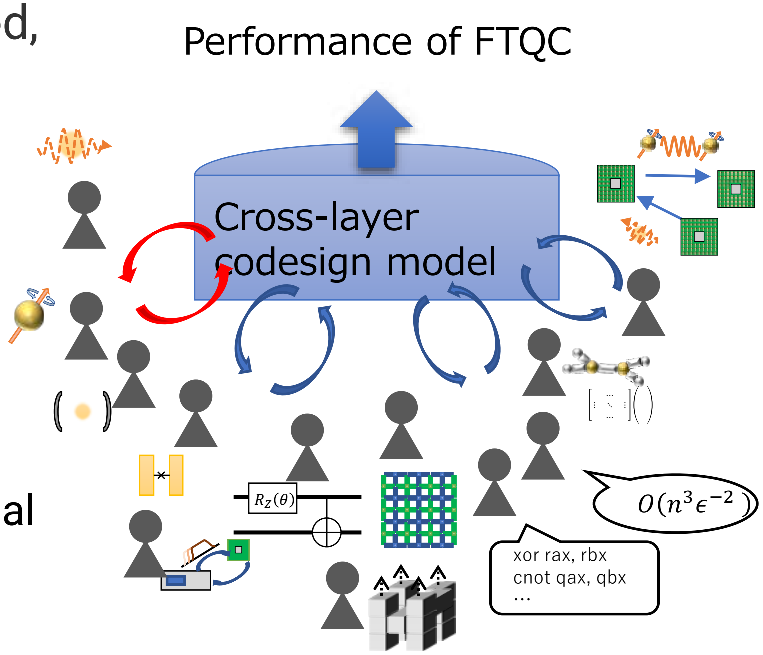
・As the model extends its scope, it may serve as an adviser in determining the direction of the Program.

Optimization over multiple layers may reveal a true bottleneck

Comparison of different approaches through the model may clarify pros and cons.



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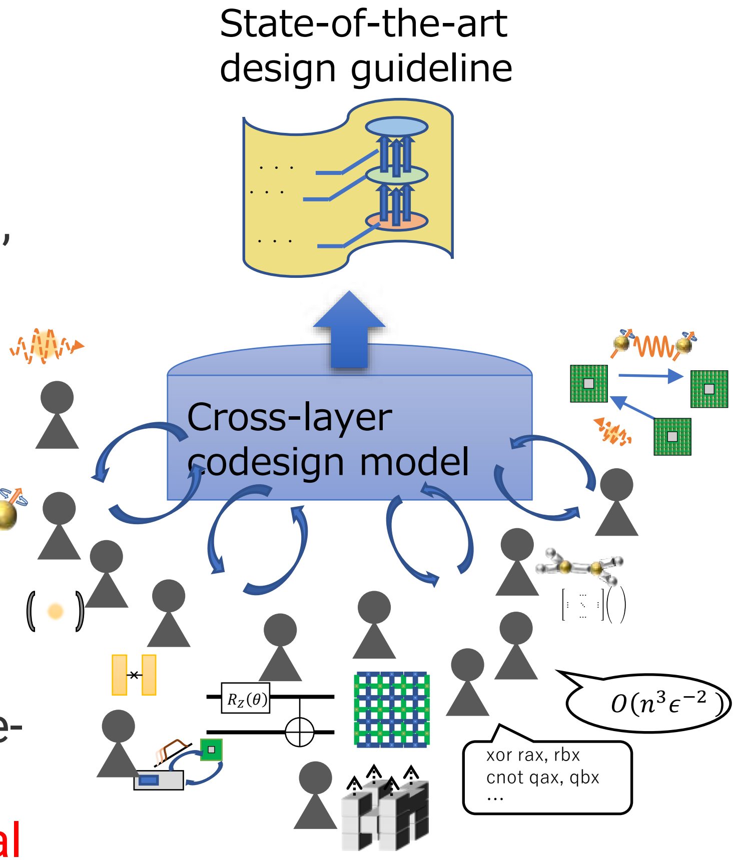
・As the model extends its scope, it may serve as an adviser in determining the direction of the Program.

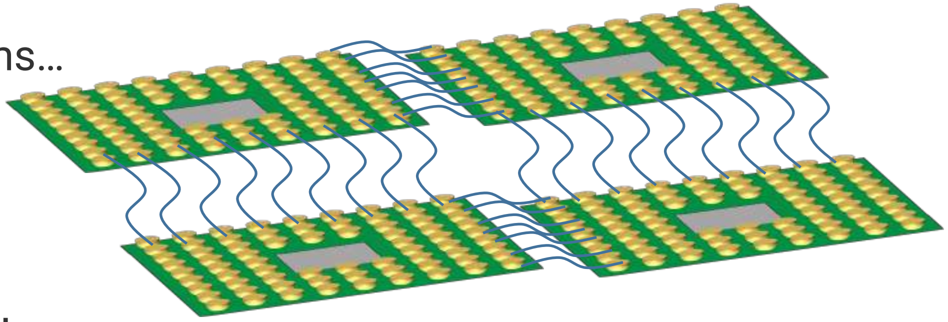
・The model can eventually put together the state-of-the-art results in each layer to produce an optimized design of FTQC, serving as a dynamical blueprint.



Distributed computing systems

- Optional for some physical systems, inevitable for others.

  Chip size constraints, heating problems…



- Requires good interconnectors
- Decoherence, latency, lower connectivity
- Compilation tends to be complicated

- Integration issues are mitigated
- Heterogeneous node types: possibility of cherry-picking
- Flexible connection geometry
- Non-local encoding may robust against burst errors and control errors.

Participants to the project

Subject 1: Cross-layer codesign model


Yuuki Tokunaga
(NTT)

Subject 2: Hardware-specific theories


Yasuhiro Tokura
(U of Tsukuba)


Kazuki Koshino
(Tokyo Medical & Dental U)


Masato Koashi
(U of Tokyo)


Franco Nori
(RIKEN)

Subject 3: Quantum error correction methods

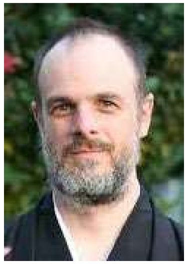

Keisuke Fujii
(Osaka U)


Kae Nemoto
(NII)

Participants to the project

Subject 4: Distributed architecture

Koji Azuma
(NTT)



Rodney Van Meter
(Keio U)

Subject 5: Exploratory challenges

Tomoyuki Morimae
(Kyoto U)

Takanori Sugiyama
(U of Tokyo)

Hiroyasu Tajima
(U of Electro-Communications)

Shumpei Masuda
(AIST)