Orchestrating a brighter world NEC

2021年4月23日
9:10-9:30
Moonshot International Symposium for Goal 6

MOONSHOT
RESEARCH & DEVELOPMENT PROGRAM

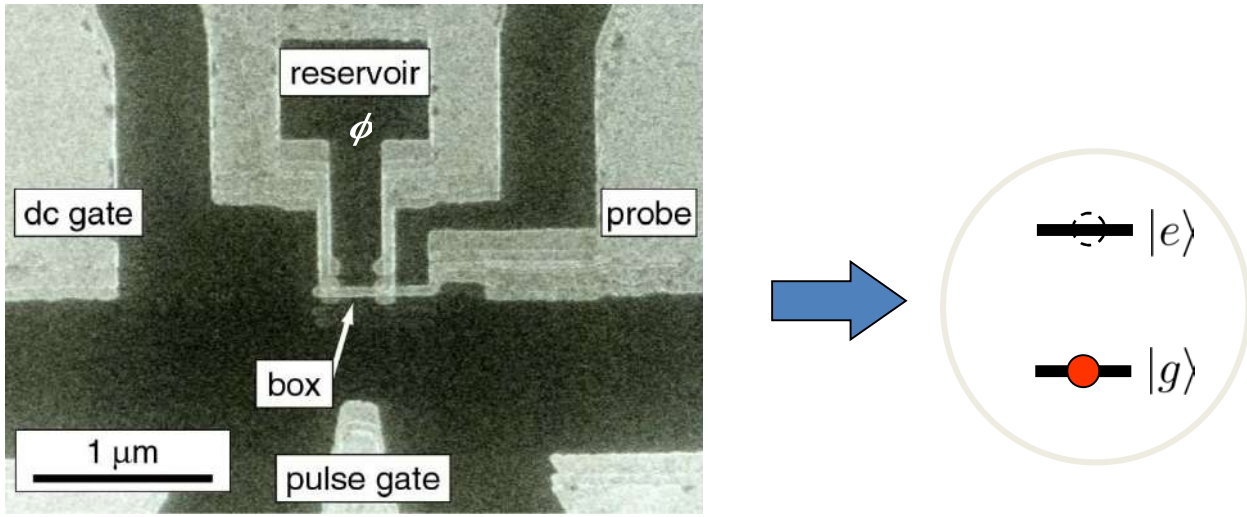
# Development of Integration Technologies for Superconducting Quantum Circuits

System Platform Research Laboratories
NEC Corporation
Tsuyoshi Yamamoto

# Table of Contents

# Superconducting qubit

- electric circuit made of superconductors and Josephson junctions
- a nonlinear oscillator with ~5 GHz resonance frequency
- operated at ~10 mK using a dilution refrigerator
- lithographically fabricated (⇔ decoherence)
- design flexibility (⇔ non uniformity)




Y. Nakamura et al., Nature **398**, 786 (1999).

# Quantum supremacy

Arute *et al.*, Nature **574**, 505 (2019).

Article

## Quantum supremacy using a programmable superconducting processor

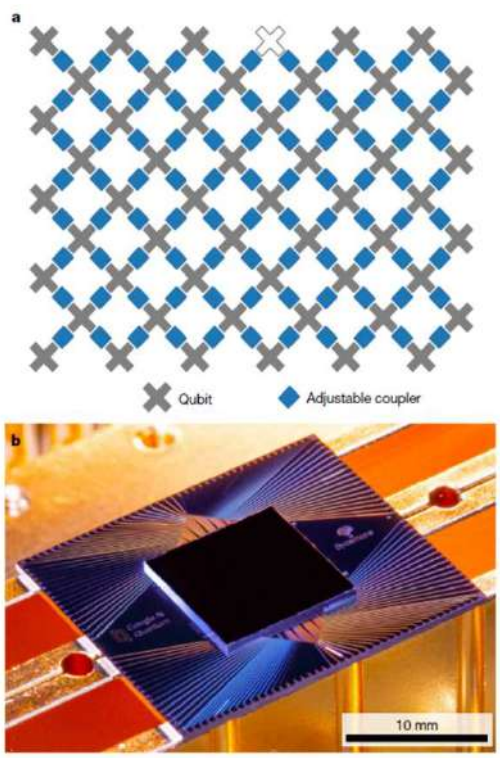
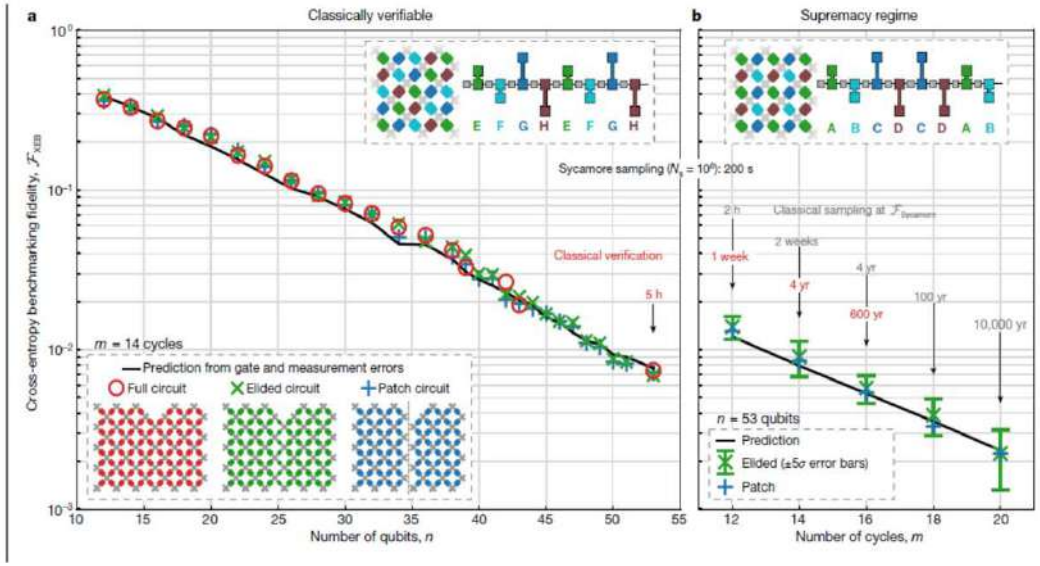



**Fig. 1 | The Sycamore processor. a**, Layout of processor, showing a rectangular array of 54 qubits (grey), each connected to its four nearest neighbours with couplers (blue). The inoperable qubit is outlined. **b**, Photograph of the Sycamore chip.




In reaching this milestone, we show that quantum speedup is achievable in a real-world system and is not precluded by any hidden physical laws. Quantum supremacy also heralds the era of noisy intermediate-scale quantum (NISQ) technologies[15]. The benchmark task we demon-

# Toward realization of fault-tolerant QC

- Two main problems in hardware development:
  - required large number of physical qubits

| Physical qubit error rate | $10^{-3}$ | $10^{-6}$ | $10^{-9}$ |
|---|---|---|---|
| Physical qubits per logical qubit | 15,313 | 1,103 | 313 |
| Total physical qubits in processor | $1.7 \times 10^6$ | $1.1 \times 10^5$ | $3.5 \times 10^4$ |
| Number of T state factories | 202 | 68 | 38 |
| Number of physical qubits per factory | $8.7 \times 10^5$ | $1.7 \times 10^4$ | $5.0 \times 10^3$ |
| Total number of physical qubits including T state factories | $1.8 \times 10^8$ | $1.3 \times 10^6$ | $2.3 \times 10^5$ |

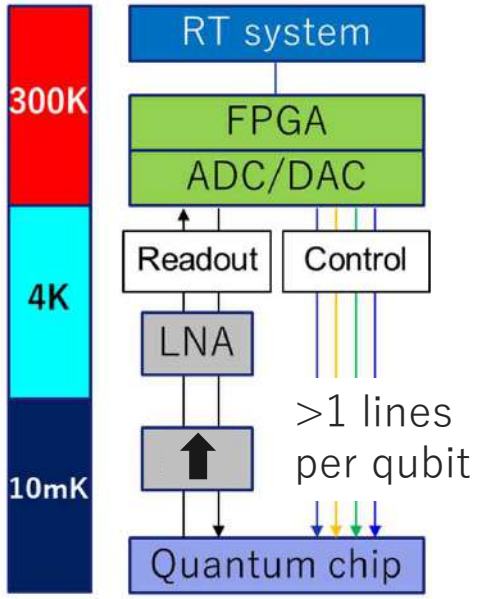
TABLE 3.1 Estimates of the Resource Requirements for Carrying Out Error-Corrected Simulations of a Chemical Structure (FeMoco in Nitrogenase) Using a Serial Algorithmic Approach for Hamiltonian Simulation and the Surface Code for Error Correction

Quantum Computing: Progress and Prospects (2019)

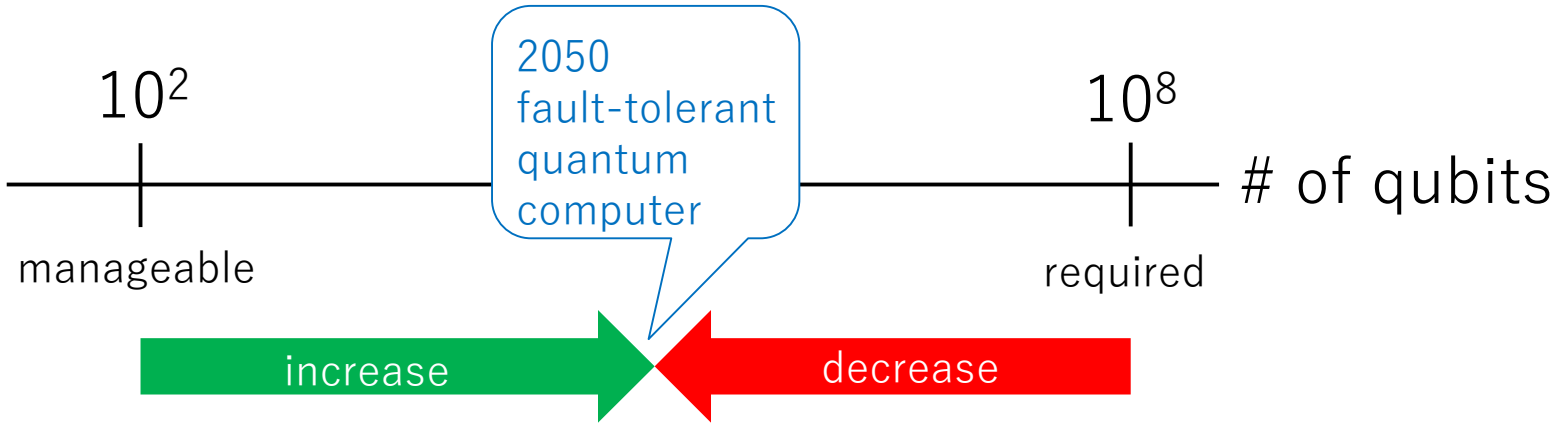
$\sim 10^8$ qubits?

  - not scalable wiring & electronics
    - >1 coax line per qubit from RT to mK for control
    - bulky μ-wave components (amplifier, isolator) for readout

$< \sim 10^2$ qubits?



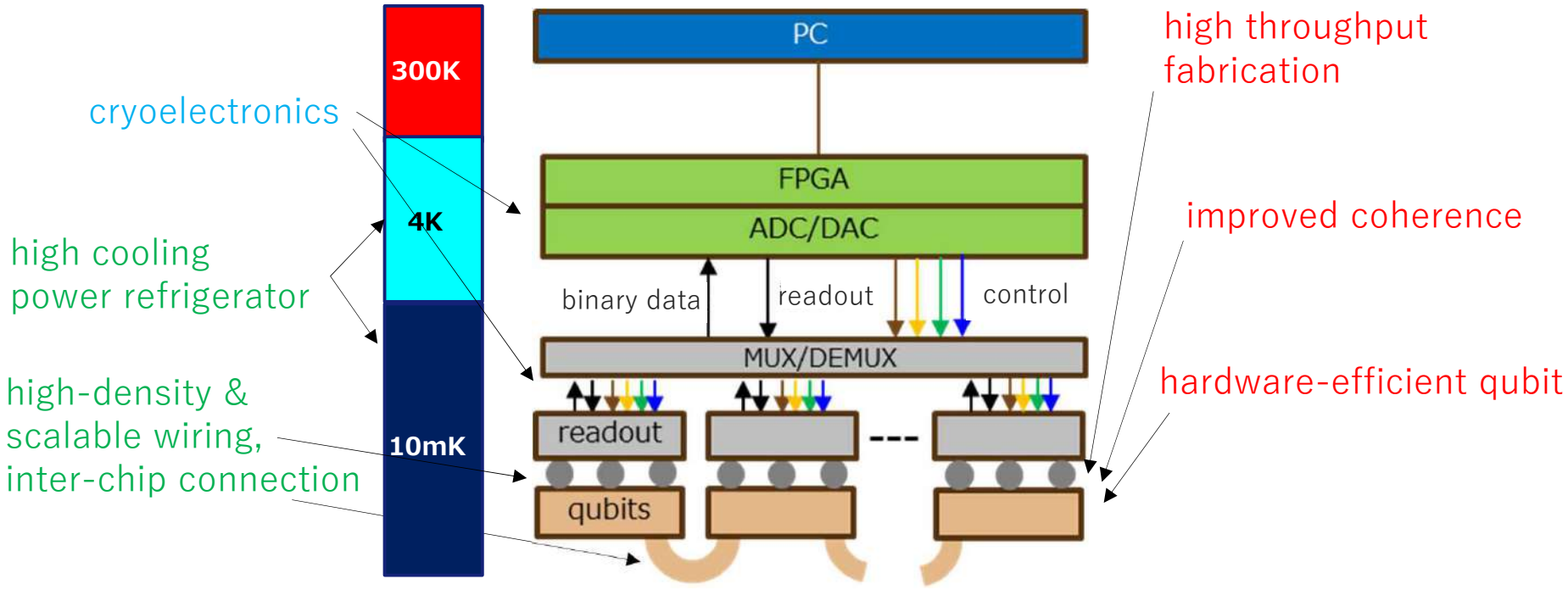
# Required technologies




- cryoelectronics
- high-cooling-power refrigerator
- high-density wiring
- chip-to-chip interconnection
- …

- improved coherence
- gate optimization
- hardware-efficient QEC scheme
- …

# Research themes of the project




1. SC qubits for fault-tolerant quantum computing
2. Hardware system for integrated qubits
3. Electronics for quantum error correction

# 1. SC qubits for fault-tolerant quantum computing

A) Improving coherence of SC qubits

- Tsuyoshi Yamamoto, NEC Corporation

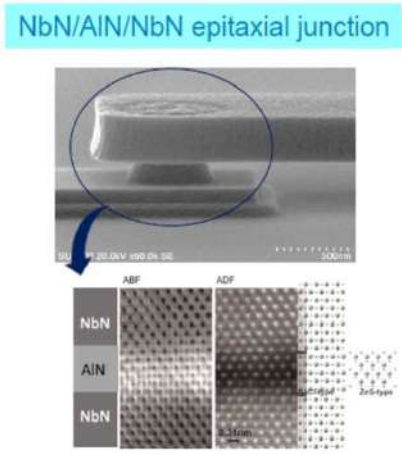
- Kunihiro Inomata, National Institute of Advanced Industrial Science and Technology

- Kazuki Koshino, Tokyo Medical and Dental University

B) Development of SC qubits with epitaxially-grown Josephson junctions

- Fumiki Yoshihara, National Institute of Information and Communications Technology

- Masamitsu Tanaka, Nagoya University



# 1. SC qubits for fault-tolerant quantum computing

C) Development of SC qubit fabrication process with high throughput and uniformity

- Satoru Odate, Nikon Corporation

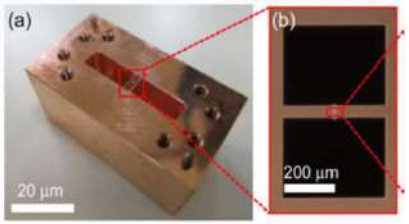
AIST Super Clean Room

D) Bosonic qubits with superconducting resonators

- Shiro Saito, NTT Basic Research Laboratories

- Atsushi Noguchi, Institute of Physical and Chemical Research

- Jaw-Shen Tsai, Tokyo University of Science




Abdurakhimov et al., APL **115**, 262601 (2019).

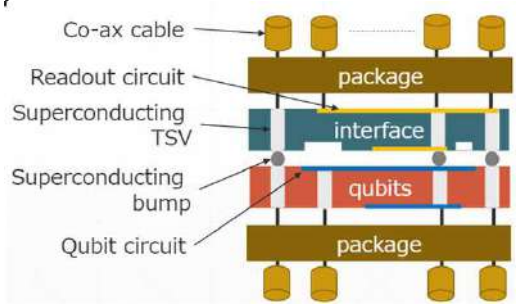
# 2. Hardware system for integrated qubits

A) Development of hybrid qubit module

- Shinichi Yorozu, Institute of Physical and Chemical Research

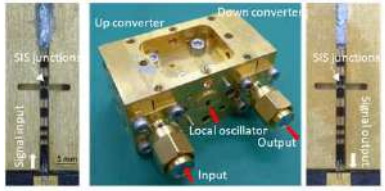
B) Development of refrigeration system specialized for quantum computing

- Masamichi Saitoh, ULVAC CRYOGENICS Inc.




- Yuya Fujiwara, ULVAC Inc.

C) Development of low-noise microwave amplifier based on superconducting SIS mixers




SIS mixer

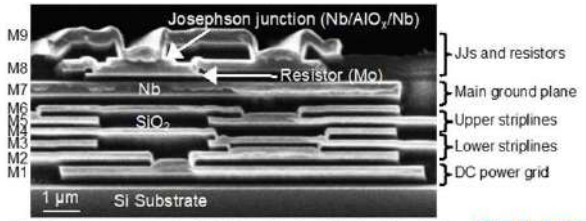
- Yoshinori Uzawa, The National Astronomical Observatory of Japan

- Akira Kawakami, National Institute of Information and Communications Technology

# 3. Electronics for quantum error correction

A) Study of single flux quantum circuits for control and readout of qubits

- Masamitsu Tanaka, Nagoya University




S. Nagasawa et al. *IEICE* **E97-C** (2014) 132-140.

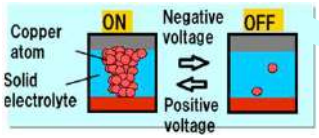
B) Study of cryo-LSI for control and readout of qubits

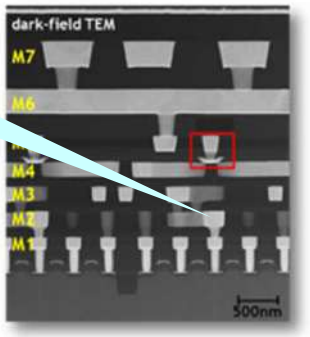
- Munehiro Tada, NanoBridge Semiconductor, Inc.

- Ken Uchida, the University of Tokyo

- Hiroki Ishikuro, Keio University

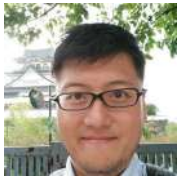
NanoBridge



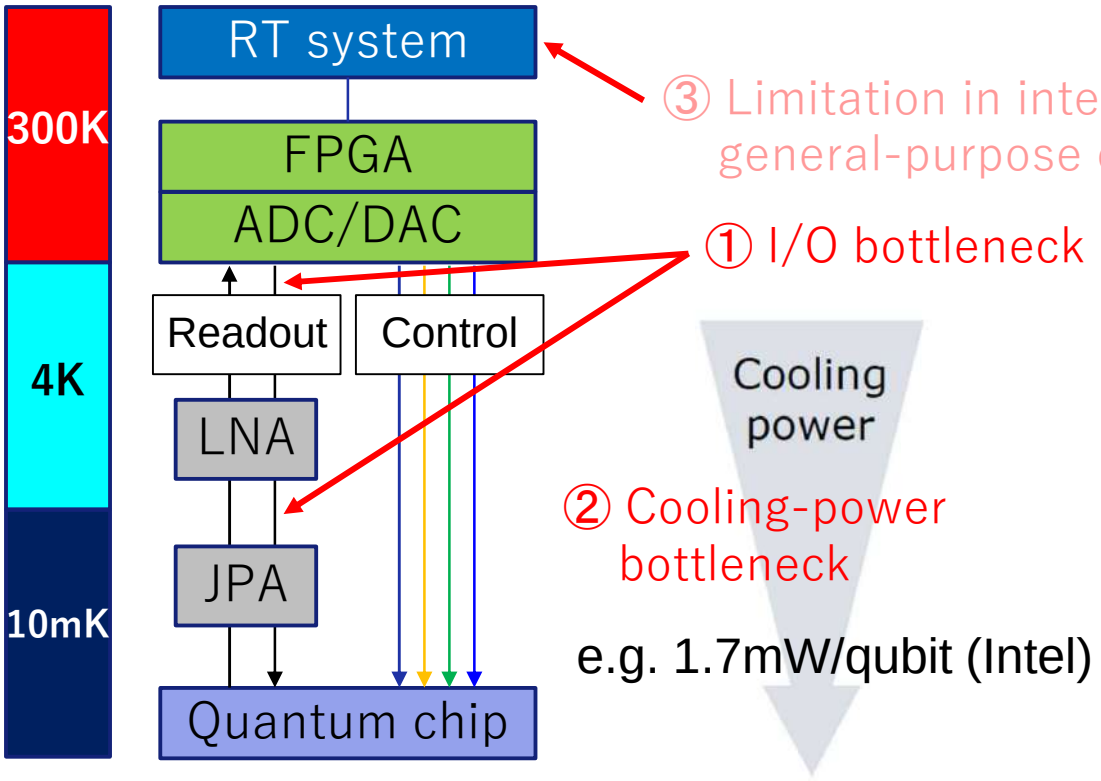

C) Study of digital microwave electronics for control of superconducting quantum computers

- Makoto Negoro, Osaka University



# Aims of Research in Electronics for QEC

- Solve the I/O and cooling-power bottlenecks by using single-flux-quantum (SFQ) logic and NanoBridge LSI's.
- Development of low-latency, scalable microwave electronics.

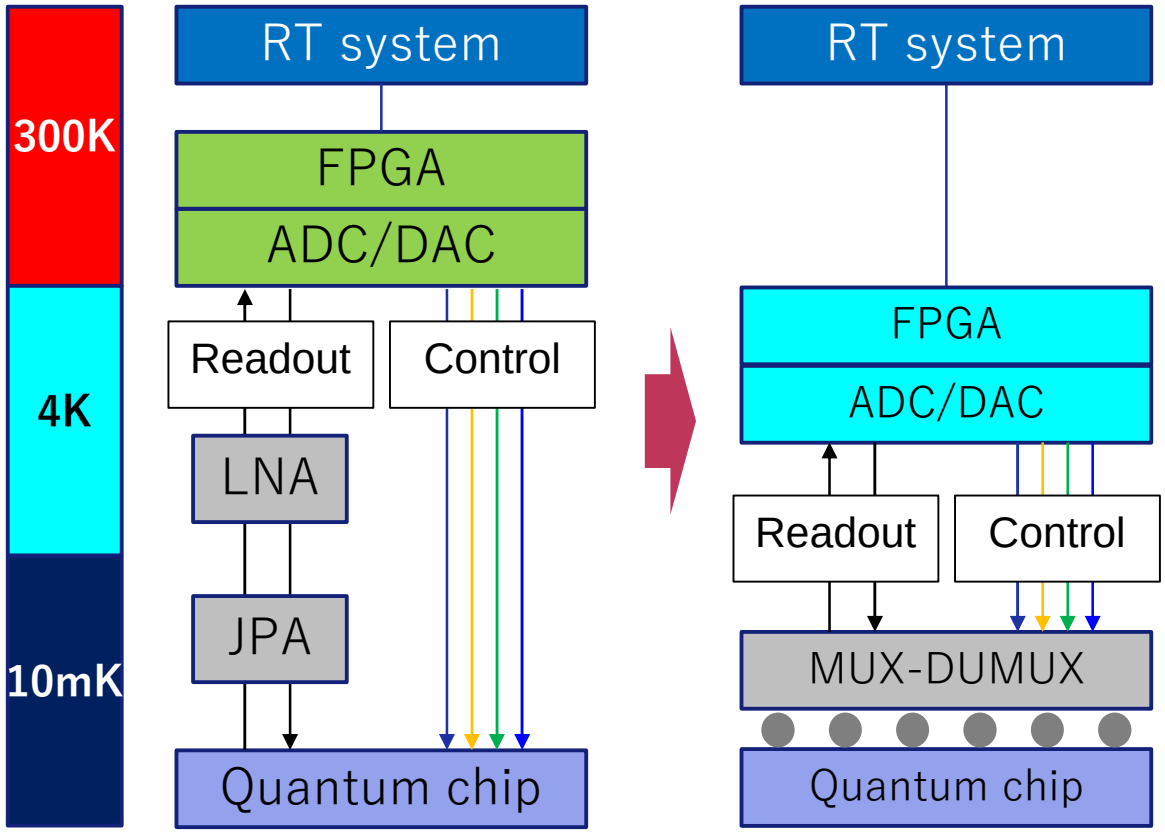


# Approach

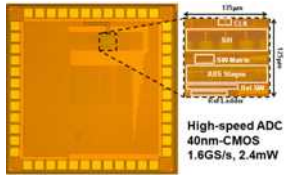
- Co-optimization of SFQ, NanoBridge, cryo-CMOS, and FPGA technologies.

Microwave electronics

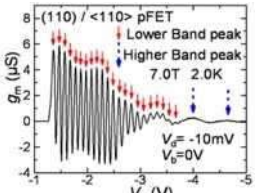
Osaka U.



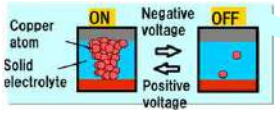

Cryo-CMOS, analog components



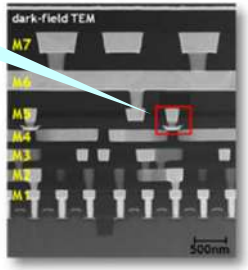

Keio U.




U. Tokyo




NanoBridge FPGA

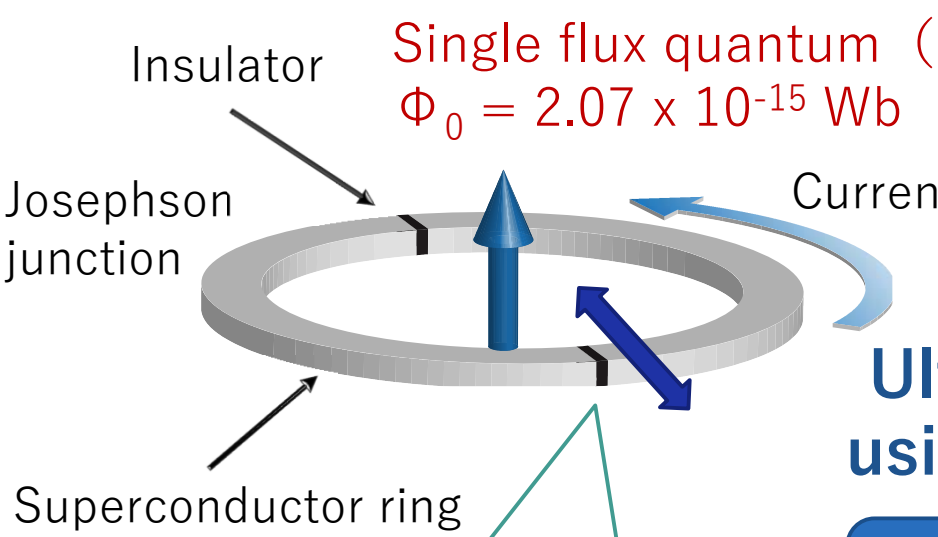


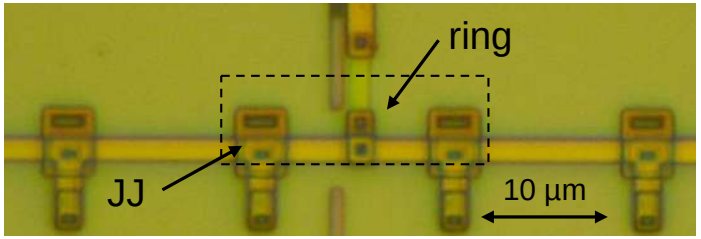

NBS Inc.

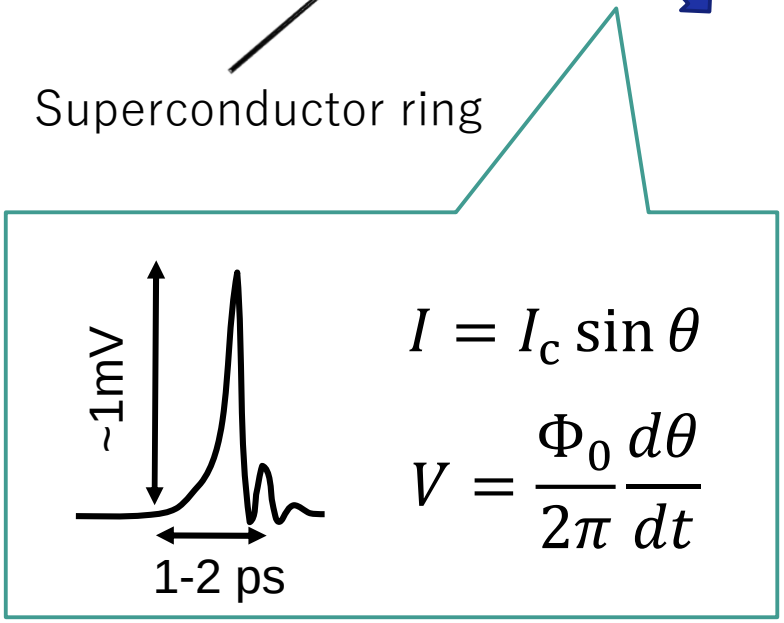
Superconductor SFQ

Nagoya U.

# Single-Flux-Quantum Logic Circuits



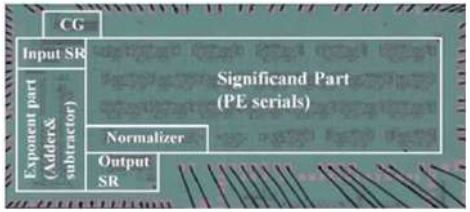

## Ultra high-speed digital LSIs using quantized magnetic flux

- ❖ Zero-mass information carrier
- ❖ No recharge process

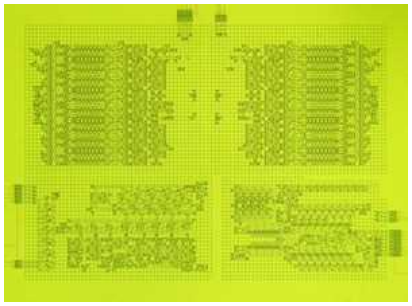
- 100-GHz-class clock operation
- Low-power (< 1/1000 of CMOS)
- Interconnects at the speed of light
- Scaling law

# SFQ LSI's demonstrated by Nagoya Univ. group

Main challenge:
Circuit optimization for 10 mK operation

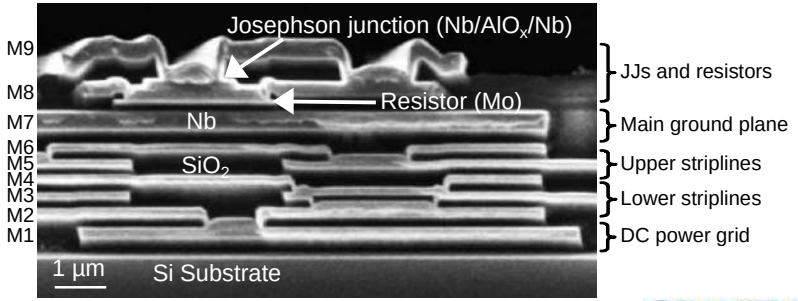



**59-GHz FP Multiplier**
18,766 JJs
X. Peng, *IEEE TAS 2015*

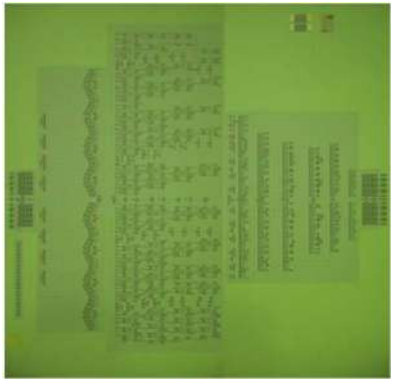


**50-GHz Processor w/ RAM**
10,603 JJs
R. Sato, *IEEE TAS 2017*

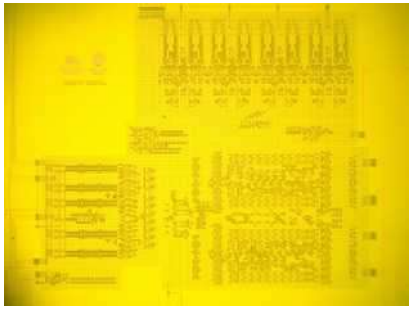
Nb 9-layer Device (AIST ADP2)




S. Nagasawa et al. *IEICE* **E97-C** (2014) 132-140.



**48-GHz 8-bit Multiplier**
20,251 JJs
I. Nagaoka, *ISSCC 2019*



**32-GHz 4-bit Processor**
23,713 JJs
K. Ishida, *VLSI 2020*

**64-GHz 8-bit Datapath**
18,448 JJs
R. Kashima, *ASC 2020*

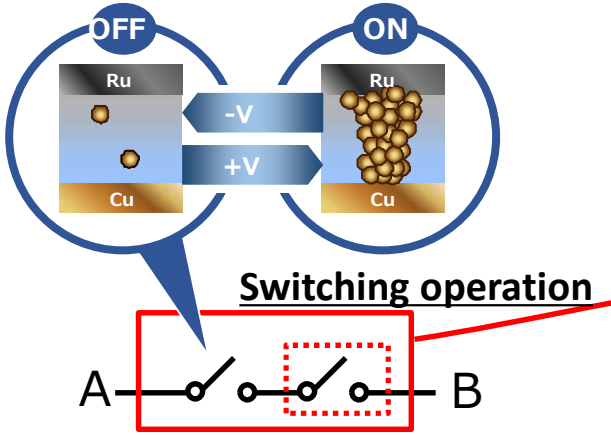
**52-GHz 0.1-mW Multiplier**
3,067 JJs
I. Nagaoka, *ASC 2020*

# NanoBridge™

**Technology**
Metallic-bridge Switching Device

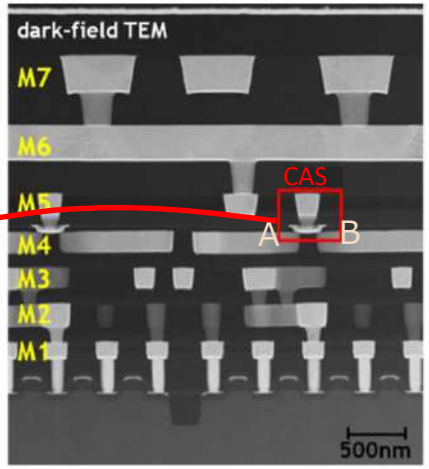
**Application**
Routing Switch
Nonvolatile-memory

**Advantage**
Low-power, Rad-hard
High-density




CAS: Complementary atom switch

**Cross sectional view**

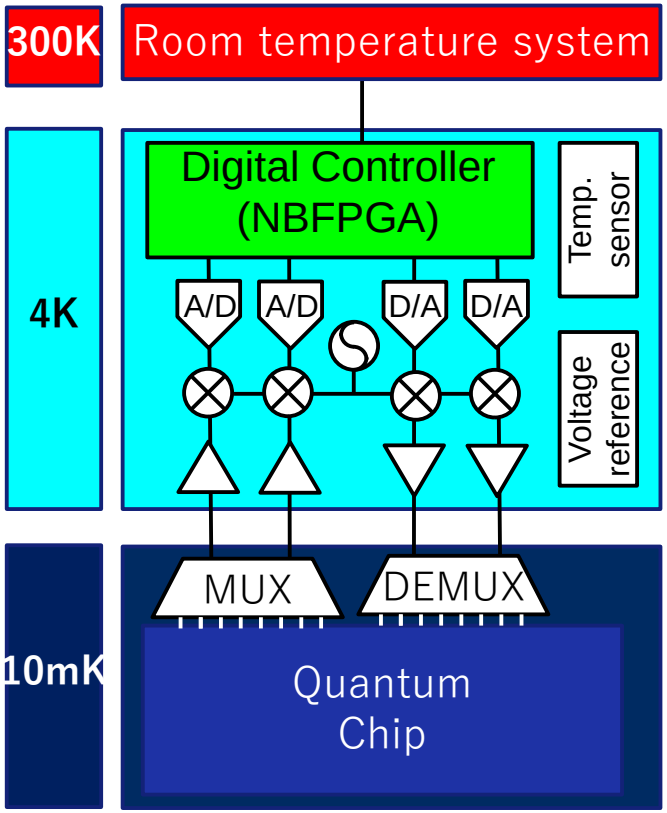



**NBFPGA**

Switching operation at 10 K has been confirmed.

# Research and Development Plan

- Build SFQ-based scalable control and readout electronics operating near qubits.




## R & D targets (5 year)

- Qubit control by SFQ demultiplexer
- Demonstration of SFQ circuits (at 10 mK) controlled by NanoBridge FPGAs

1) Ultralow-power SFQ circuit technology (1/100 compared to 4-K design)
2) Demonstration of digital demultiplexer
3) Build qubit control systems using SFQ and NanoBridge LSIs
4) Study on SFQ-friendly qubit readout

# Summary

- In order to realize fault-tolerant superconducting quantum computer, we need to increase the number of manageable qubits and to decrease the number of required qubits both by orders of magnitude.

- In this project, we will develop hardware technologies required for scaling up the circuit of superconducting qubits more than 100, and reducing the hardware complexity.
  - SC qubits for fault-tolerant quantum computing
  - Hardware system for integrated qubits
  - Electronics for quantum error correction

- We will collaborate with Q-LEAP project (Prof. Nakamura), which targets the ~100 qubit circuit for the NISQ application, to realize further scale-up smoothly.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