

Survey of Technological Issues in Device Fabrications Processes for Gallium Oxide as a Next-Generation Widegap Semiconductor (Vol. 2): Clarification of Energy Band Diagram of Single-Crystalline Gallium Oxides

Summary

High quality crystals has recently become available for gallium oxide (Ga_2O_3), which is attracting attention as one of the next generation wide gap semiconductor device materials. In this proposal, the energy band diagram of Ga_2O_3 MOS capacitor was clarified by investigating the surface of $\beta\text{-Ga}_2\text{O}_3$ single crystal by means of ultraviolet photoelectron spectroscopy. The interface fixed charge density (N_{int}) of the fabricated capacitors was also estimated experimentally, and it was found that the N_{int} was suppressed to $\sim 1 \times 10^{11} \text{ cm}^{-2}$ with an annealing time of more than 1 hr at 1000°C . It was shown from these findings that the precise understanding of the energy band diagram is important for evaluation of device characteristics.

Proposals for Policy Development

- This time, the energy band diagram of gallium oxide (Ga_2O_3) was investigated, and the device characteristics were evaluated. The obtained interface fixed charge density (N_{int}) and other parameters are not only necessary for improving the device processes, but also indispensable for the exact prediction of device operation and the device design.
- To establish the next-generation widegap semiconductor device technology, it is important not only to accelerate the demonstration of device operation, but also to proceed basic researches for understanding the fundamental properties such as band structure, and the chemical properties such as reactivity, in order to develop a knowledge base available for engineers and researchers working on the properties of those semiconductor materials.

1. Clarification of $\beta\text{-Ga}_2\text{O}_3$ energy band diagram by means of UPS spectrum
 UV photoelectron spectroscopy (UPS) analysis was performed on $\beta\text{-Ga}_2\text{O}_3(001)$ wafers obtained by recent growth technology for large-area wafer (Fig. 1). The low kinetic energy end (cut-off) and the high kinetic energy end (valence band maximum) of the UPS spectrum were found to be 3.5 eV and 16.5 eV by linear extrapolation respectively, and the valence band maximum energy level, E_V , was estimated is $8.15 \pm 0.02 \text{ eV}$ below the vacuum level. Since the band gap of $\beta\text{-Ga}_2\text{O}_3$ is 4.7 - 4.8 eV [1], it was estimated that the conduction band minimum energy level, E_C , is 3.4 - 3.5 eV deep below the vacuum level.

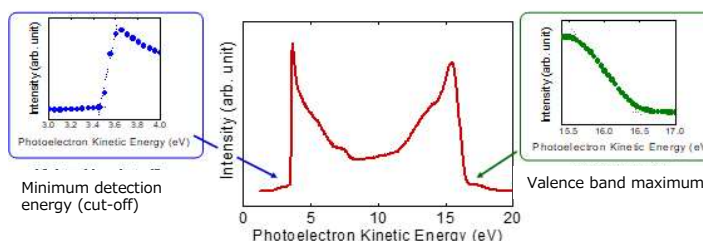


Fig. 1 UPS spectrum on the surface of $\beta\text{-Ga}_2\text{O}_3(001)$ wafer and enlarged views of the spectrum near the minimum detection energy region (left) and near the valence band maximum energy region (right)

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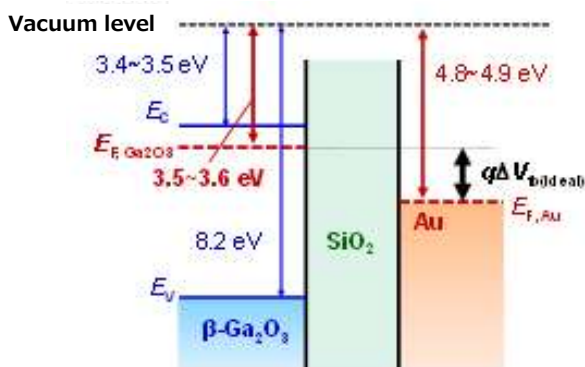


Fig. 2 Energy band diagram of the $\beta\text{-Ga}_2\text{O}_3(001)$ wafer and the fabricated MOS capacitor, referred to the vacuum level.

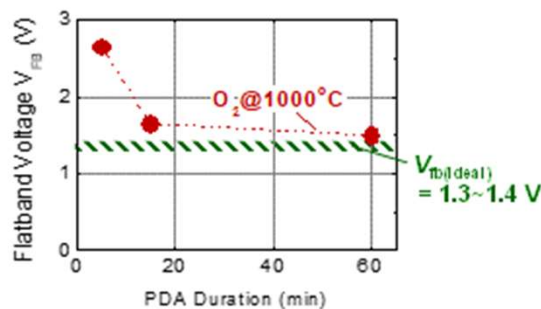


Fig. 3 Relationship between V_{fb} and oxygen annealing duration for Au/ SiO_2 (film thickness of about 30 nm)/ $\beta\text{-Ga}_2\text{O}_3$ MOS capacitors

2. Re-verification of device characteristics by estimating Fermi level

Since the difference between the Fermi level $E_{F, \text{Ga}_2\text{O}_3}$ and E_C was calculated to be 0.1 eV, the Fermi level of $\beta\text{-Ga}_2\text{O}_3(001)$ epitaxial film $E_{F, \text{Ga}_2\text{O}_3}$ was estimated to be 3.5 - 3.6 eV deep below the vacuum level. These data are shown in the energy band diagram in Fig. 2.

Finally, the interface fixed charge density (N_{int}) was estimated from CV characteristics of the fabricated MOS capacitors. The fabricated MOS capacitors, Au/ SiO_2 (film thickness of about 30 nm)/ $\beta\text{-Ga}_2\text{O}_3$, were used to measure the flat band voltage (V_{fb}) by varying the oxygen annealing duration from 5 minutes to one hour under $1,000^\circ\text{C}$ (Fig. 3). The N_{int} estimated on the basis of the V_{fb} shift from the ideal value ($V_{\text{fb(ideal)}}$) determined using $E_{F, \text{Ga}_2\text{O}_3}$ was minimized to up to $1 \times 10^{11} \text{ cm}^{-2}$ under the condition of annealing duration of one hour. It was clarified from the fabricated MOS capacitor, that the annealing at $1,000^\circ\text{C}$ is effective in reducing the interface fixed charges.

[1] S. J. Pearton, J. Yang, P. H. Cary, F. Ren, J. Kim, M. J. Tadjer, and M. A. Mastro, Appl. Phys. Rev. 5,011301, 2018.