

革新的コンピューティング技術の開拓
2020年度採択研究代表者

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Tran Thi Hong

大阪公立大学 大学院情報学研究科
講師

Society 5.0 向け超低消費電力ブロックチェーンアクセラレータの開発

研究成果の概要

In this school year, we have conducted research in both hardware and software aspects of Blockchain technology.

In the aspect of hardware development, we have developed and evaluated several accelerators for securing Blockchain network, such as: Flexible and Scalable BLAKE/BLAKE2 Coprocessor, A Compact Scrypt core, A Coarse Grained Reconfigurable Architecture for SHA-2 Accelerator. The research results have been published in several international transactions such as IEEE Design and Test, IEEE Access; and presented in international conferences as will be listed below.

In the aspect of software development, we have developed three main decentralized applications (DApps), such as: Scorechain for smart campus, Vacchain for tracking vaccine, and SmartCV for providing reliable resume resource of talents. The research results have been published in the Highlight of MDPI Journal of *Cryptography*. Some researches are on progress and will be submitted for publication in next school year.

代表的な原著論文情報

I. International Journal

1. P. H. Luan, T. H. Tran, V. T. Duong Le and Y. Nakashima, "Flexible and Scalable BLAKE/BLAKE2 Coprocessor for Blockchain-based IoT Applications", IEEE Design&Test. (accepted)
2. Atsuki Koyama, Van Chuong Tran, Manato Fujimoto, Vo Nguyen Quoc Bao, and **Thi Hong Tran***, "A Decentralized COVID-19 Vaccine Tracking System Using Blockchain Technology," Journal of *Cryptography* **2023**, 7(1), 13; <https://doi.org/10.3390/cryptography7010013>. [Link](#)
3. Van Duy Tran, Duc Khai Lam*, and **Thi Hong Tran**, "Hardware-Based Architecture for DNN Wireless Communication Models," Journal of *Sensors* **2023**, 23(3), 1302; <https://doi.org/10.3390/s23031302>. [Link](#)
4. H. L. Pham, **T. H. Tran***, V. T. D. Le and Y. Nakashima, "Compact Message Permutation for a Fully Pipelined BLAKE-256/512 Accelerator," in IEEE Access, 2022, doi: 10.1109/ACCESS.2022.3181410, June 8th 2022. [Link](#)

II. International Conference

1. Vu Trung Duong Le, Hoai Luan Pham, **Thi Hong Tran**, and Yasuhiko Nakashima: "CSIP: A Compact Scrypt IP design with single PBKDF2 core for Blockchain mining", 2022 35th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design

(SBCCI), Porto Alegre, Brazil, 2022, pp. 1-6, doi: 10.1109/SBCCI55532.2022.9893217 (2022)

2. **【Best Track Award on Track SoC, NoC and Reconfigurable Systems】**Hoai Luan Pham, Thi Hong Tran, Vu Trung Duong Le, and Yasuhiko Nakashima: "A Flexible and Energy-Efficient BLAKE-256/2s Co-Processor for Blockchain-based IoT Applications", 2022 35th SBC/SBMicro/IEEE/ACM Symposium on Integrated Circuits and Systems Design (SBCCI), Porto Alegre, Brazil, 2022, pp. 1-6, doi: 10.1109/SBCCI55532.2022.9893257. (2022)
3. Hoai Luan Pham, Thi Hong Tran, Vu Trung Duong Le, and Yasuhiko Nakashima: "A High-Efficiency FPGA-Based BLAKE-256 Accelerator for Securing Blockchain Networks", IEEE International Midwest Symposium on Circuits and Systems, DOI: [10.1109/MWSCAS54063.2022.9859292](https://doi.org/10.1109/MWSCAS54063.2022.9859292) Aug. 22nd (2022), <https://ieeexplore.ieee.org/document/9859292>
4. Hoai Luan Pham, Thi Hong Tran, Vu Trung Duong Le, and Yasuhiko Nakashima: "A Coarse Grained Reconfigurable Architecture for SHA-2 Acceleration", 2022 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), Lyon, France, 2022, pp. 671-678, doi: 10.1109/IPDPSW55747.2022.00117. Link: <https://ieeexplore.ieee.org/document/9835347>