革新的コンピューティング技術の開拓
2020 年度採択研究者

2020 年度
年次報告書

TRAN THI HONG

Nara Institute of Science and Technology, Division of Information Science
Assistant Professor

Ultra Low Power Consumption Blockchain Accelerator for Society 5.0

「Society 5.0 向け超低消費電力ブロックチェーンアクセラレータの開発」

§1. 研究成果の概要

From 2020/11 to 2021/3, I have focused on two main tasks: 1) develop high processing rate low power consumption hardware architectures for cryptography hash functions SHA-256 and SHA-3 which are required to secure blockchain networks, and 2) build blockchain software platform. Task 1 has achieved some achievement, and task 2 is on progress. Notably, task 1 has proposed a multimem SHA-256 accelerator that achieves high performance at the system on chip (SoC) level. The accelerator employs three novel techniques, the pipelined arithmetic logic unit (ALU), multimem processing element (PE), and shift buffer in shift buffer out (SBi-SBo), to reduce the critical path delay and significantly increase the processing rate. Experiments on a field-programmable gate array (FPGA) and an application-specific integrated circuit (ASIC) show that the proposed accelerator achieves significantly better processing rate and hardware efficiency than previous works. The accelerator accuracy is verified on a real hardware platform (FPGA ZCU102). The accelerator is synthesized and laid out with 180 nm complementary metal oxide semiconductor (CMOS) technology with a chip sized 8.5mm×8.5mm, consumes 1.86 W, and provides a maximum processing rate of 40.96 Gbps at 80 MHz and 1.8 V. With FPGA Xilinx 16 nm FinFET technology, the accelerator processing rate is as high as 284 Gbps. A part of SHA-256 accelerator has been applied for Japan patent. The SHA-256 accelerator results have been accepted to present in international conferences, and published in IEEE Access journal.

【代表的な原著論文情報】

[1] **Thi Hong Tran**, Hoai Luan Pham, and Yasuhiko Nakashima, "A High-Performance Multimem SHA-256 Accelerator for Society 5.0," in IEEE Access, vol. 9, pp. 39182-39192, 2021, doi: 10.1109/ACCESS.2021.3063485.

[2] **Thi Hong Tran**, Yasuhiko Nakashima,“処理要素、その制御方法および制御プログラム、並びに処理装置,” 日本特許庁, 特願 2021-009164, Jan. 2021.

[3] Van Dai Phan, Hoai Luan Pham, **Thi Hong Tran**, Yasuhiko Nakashima, “High Performance Multicore SHA-256 Accelerator using Fully Parallel Computation and Local Memory,” IEEE Symposium on Low-Power and High-Speed Chips and Systems (COOL Chips 24), April 2021. (to be published)

[4] Tri Dung Phan, **Thi Hong Tran**, Yasuhiko Nakashima, “Design and Evaluation of High Performance SHA-3 System on Chip for Society 5.0,” IEEE Symposium on Low-Power and High-Speed Chips and Systems (COOL Chips 24), April 2021. (poster)

[5] **Thi Hong Tran**, “High Performance Blockchain Accelerator (BCA) for Society 5.0,” online invited talk in MOBI Innovation Lecture series, Los Angeles USA, March 2021, link: https://www.youtube.com/watch?v=DXfembfZDyA