Ultra-Low-Power Data-Driven Networking System

Hiroaki NISHIKAWA
Department of Computer Science,
Graduate School of Systems and Information Engineering, University of Tsukuba
Tsukuba Science City, Ibaraki 305-8573 Japan

Reducing power consumption in networking system is one of the most crucial issues to maintain communication capability for sufficient time in emergency. And at the same time, keeping connectivity by avoiding any congestion is essential in networking architecture. Our research project is therefore developing ultra-low-power data-driven networking system (ULP-DDNS) which can provide longer lifetime or stronger dependability even under severe power budget and traffic condition. That is, each networking node can work well by consuming the minimum and essential power without any runtime overheads such as overload avoidance overhead of multiprocessing. The key contribution of our project to ultra-low-power technology is to ultimately utilize passive data-driven principle throughout ad hoc networking scheme, data-driven chip multiprocessor platform and its VLSI realization, in terms of perfect elimination of any control overheads at every layer of the system. As a result of current estimations, our ULP-DDNS can perform with 1/300 power of the present.

Traffic Reduction Schemes of Ad hoc Network

Our project has been studying information discovery, authentication and information forwarding to reduce traffic in ad hoc network. Among them, a load-aware flooding scheme invented in our project can avoid congestion by discarding redundant packets by observing local load of each node. At present, our schemes proposed reduce the traffic to 1/10 and reduce power consumption to 1/10 in conventional networks.

Optimized Data-Driven Implementation of UDP/IP

Our UDP/IP implementation in the data-driven processor ULP-CUE shortens turn-around time by parallelizing header processing and datagram manipulation. Furthermore, our project proposed an optimized functional circular pipeline structure to efficiently execute unary-operations frequently encountered in the UDP/IP by bypassing firing control function.

VLSI Realization of ULP-DDCMP

Our project has already fabricated ULP-DDCMP (Data-Driven Chip Multiprocessor) with 65nm CMOS 7 ML process. ULP-DDCMP consists of 4 ULP-CUEs working as a data-driven chip multiprocessor core. The circular pipeline introduced in ULP-CUE makes it possible to bypass the firing control stage which is unused for unary-operations occupying more than 80% of the UDP/IP program. As a result, the amount of power consumption and the execution time of the UDP/IP program can be reduced drastically. Furthermore ULP-DDCMP can reduce power consumption by function distribution and load-sharing among chip multiprocessor cores. That is, when load is lower situation, core level power gating (PG) is effective to reduce power consumption by cutting leak current. In another situation, core level dynamic voltage scaling (DVS) achieves total low power execution among chip multiprocessor cores. In our estimations, demanded maximum concurrency of UDP/IP would be 4 and the maximum throughput in ad hoc network would be 3Gbps. The requirements can be satisfied by handling single thread on each ULP-CUE. Apparently, PG and DVS in the optimized circular pipeline are fully utilized to achieve lower power processing in the single thread execution. Furthermore, our project proposed a mechanism to avoid congestion by observing current on each ULP-CUE. In conventional mechanisms for avoiding congestion, it is necessary for each node to monitor the actual traffic processed to know own load. Fulltime monitoring traffic results in considerable overheads in the node. Our mechanism by simply observing its own current minimizes the overheads.

Self-Timed Power-Aware Elastic Pipeline:ULP-STP

We have studied an implementation of the stage-by-stage PG function which can cut leak power in empty stage by fully utilizing distributed control in self-timed elastic pipeline (STP). Each stage has PG switches which gate supply power to its logic and data latch to eliminate leakage current in idle condition. Furthermore, our project has introduced DVS control managed by current consumed in the STP. This is because the throughput is proportional to current consumption in the STP. We evaluated the effect of stage-by-stage PG and core-level DVS by implementing a prototype of ULP-STP, self-timed elastic pipeline with the PG and DVS. As a result, power consumption in 0.8V is 38% less than power consumption in 1.2V, and the PG function achieved 93% reducing leak power in the empty stages. In order to fully utilize the fruitful results of the PG and DVS, our project has studied a fine-grain power control scheme to avoid overloaded conditions by monitoring current consumed in the ULP-CUE.

Evaluations for Low Power Consumption and Further Works

In parallel with developing a set of hardware boards as prototype ULP-DDNS node, a power simulator/validator has been developed to evaluate fine grain operations and power consumptions in the self-timed power-aware elastic pipeline with PID (Proportional-Integral-Derivative) control. It will be one of the most powerful tools to demonstrate effectiveness in PG and DVS functions in the ULP-DDNS. Through evaluations in the avoiding congestion scheme, our ULP-DDNS will be one of the most promising ways to keep connectivity of the communication environment in emergency.