Innovative Power Control for Ultra Low-Power and High-Performance System LSIs

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I. INTRODUCTION

The purpose of this project is to achieve drastic reduction of power consumption through tight co-operation and co-optimization between system software, architecture and circuit-level design. For this purpose, we have developed a fine grain power gating processor called Geyser and a coarse grain reconfigurable processor called SLD (Silent Large Datapath), and conducted an extensive research on low-power NoCs. This summary describes only Geyser due to the page limitation. Detailed descriptions of other topics can be found in articles [3] [4] [6] [7].

II. GEYSER: FINE-GRAINED POWER GATING PROCESSOR

Leakage power dissipation in LSI chips has been increasing exponentially with device scaling, and has grown to be a major component in the total power dissipation today. Among existing techniques to reduce leakage power, power gating is one of the most promising approaches.

So far, power gating control have been implemented at a course granularity both in terms of area and time. In contrast, we have been studying more aggressive techniques to power gate internal circuits in the microprocessor in much finer granularity at run-time. For fine-grained run-time power gating, it is important to detect/predict when and which unit should be put into sleep mode. This should be done with the help of both hardware and software because there exists dynamically or statically determined idle periods. Thus, we propose an architectural (hardware) technique to tackle idle periods caused by dynamic events and a compiler (software) technique to predict and handle statically determined idle periods. That is to say, architecture should be built in a way that it can detect the chance of power gating and appropriately put the target unit into sleep mode. Also, it should offer a suitable ISA interface to the software to enable controlling power gating from the software. Compiler should decide which functional unit to be put into sleep mode by analyzing the target source code and predict how long would the idle period of each functional unit after its use.

We apply our proposed fine-grained run-time power gating to a classic style in-order pipelined RISC CPU with standard five-stage pipeline structure which consists of Instruction Fetch(IF), Decode(ID), Execute(EX), Memory Access(MEM), and Writeback (WB). We select computational units in the EX stage as the functional units to be power gated. Fundamental control of fine-grained run-time power gating is as follows. All units except ALU are put into sleep mode automatically after finishing the operation in EX stage. When an instruction is fetched in the IF stage, the sleep controller check the fetched instruction and judge which computation unit to be used for the fetched instruction. Since it takes a certain time to wake up (approximately one cycle is assumed here) the unit, the detection must be done in the IF stage.

The leakage power is sensitive to the temperature and will increase drastically as the temperature rises. As the break-even point is influenced by the leakage power, the policy of power gating should be changed by measuring the amount of leakage current itself. Thus, we have implemented a leak monitor on the chip. Fig. 1 shows the layout of the first prototype Geyser-1. The chip size 2.1mm X 4.2mm. The black boxes are target components of fine-grained run-time power gating. Four small black boxes located near each corner are leakage monitors.

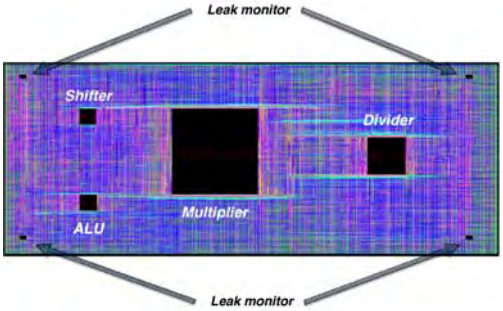

Figure 1. Layout of Geyser-1

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