Research on Ultra Low Power Media Processing SoC

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In order to realize low power media processing system on chip (SoC), Goto team focuses on designing workload allocation techniques and optimization algorithms for image processing, encryption and error correction together with optimized hardware/software implementations. It targets a 99% power reduction compared with the existing techniques for the whole multimedia communication system. For these 4 years,, techniques at the algorithm level, the hardware level and the implementation level have been designed to further improve the power efficiency for the system.

At the algorithm level: techniques to detect and predict the content difference in the compressed video data are designed, based on which the working frequency of the processor can be adjusted accordingly with the predicted variation in the computational complexity. Based on difference detection algorithm, which was developed by Waseda team to detect the content variation in the videos captured by the static cameras in the surveillance system or the TV conference system, encoding workload prediction algorithm is proposed to adjust the CPU frequency for a maximized usability under a performance constraint. By implementing the system on a multi-core platform with four cores supporting dynamic voltage and frequency scaling (DVFS) and measuring the power consumption in real-time, an average of 46% power reduction is achieved. The maximum power reduction is 78%. Moreover, region of interest (RoI) method is enhanced for TV conference systems. It reduces the RoI region (the face region) with higher accuracy, which endues the encoder with an average of 76% reduction in computational complexity.

In addition, the parallel processing algorithm of KLT Tracker was implemented on IMAP CAR for tracking the moving objects by the image sensors. Compared with the implementation on PCs, which provides only seven to eight frame per second (fps) processing speed for 320x240 images, the IMAP based implementation achieves a drastic improvement in power efficiency (power consumption is only 4% of that of a PC) by processing 640x240 images at 30 fps.

At the chip designing level: a 4096x2160 H.264/AVC video decoder is developed, which is verified to provide 60% power reduction compared with the existing solutions. The decoder achieves 60fps speed for decoding H.264/AVC High Profile compressed videos at 4096x2160. It optimized the decoding order for the macro blocks with lossless reference frame compression to reduce the bandwidth between the off-chip DRAM and the decoder engine by 38%. Implemented by SMIC 90nm technology, the chip power consumption is only 189mw at 4096x2160@60fps, which is a 55% to 64% reduction compared with the existing decoders.

For hardware oriented design: by applying power optimization algorithms for data paths including multipliers and dividers, optimized power gating methods and fine process evaluation methods for the circuits with unused clock signal input, scheduling for high-level power optimization, sharing methods, low power consumption floor planning by power-supply voltage optimization, low power design for network on chip (NoC) and low power design for processors, the whole system is to achieve 50% power reduction.

For the software oriented implementation: a processor is developed for multimedia applications to let the software executed on it can achieve much lower power consumption. The instruction sequence together with the processor architecture, which is dedicated to media processing, is built, based on which the implementation of media processing, especially H.264/AVC Intra encoding, is investigated. A parallel processing architecture is proposed for H.264/AVC Intra encoding together with the computational complexity reduction algorithms and the novel SIMD type VLIW instructions. Compared with using the existing VLIW processors, the implementation on the proposed processor provides up to 75% energy reduction (62.88% on average) while maintaining the compression efficiency.

Renesas team, joined this project since 2009, implemented the low complexity human detection algorithm, which was developed by Waseda team, on an XBridge evaluation board with a STP processor. The human detection algorithm is divided into four parts and applied on the input image at different scales. The energy consumed in detecting humans in a VGA sized image is compared between the XBridge evaluation board and a desktop PC with Core2Duo@3GHz executing the same algorithm. Comparing the platform energy consumption, XBridge platform provides 97.6% energy reduction compared with that of the PC platform. The energy consumed by the processor on XBridge is also reduced by 96.5% compared with that consumed by the processor on the PC. Overall, the implementation on XBridge platform reaches the project target by providing 10 times higher power efficiency.

As a whole system, the power can be reduced to 5-10% by introducing new algorithms, new architectures, and new design methodologies for multimedia applications, compared with the existing ones of 5 years ago.