Low-power, High-performance, Reconfigurable Processor Using Single-Flux-Quantum Circuits

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I. INTRODUCTION

Superconducting single-flux-quantum (SFQ) circuit technology is expected to be a next generation circuit technology which achieves ultra low-power computation. In this research, we develop basic technologies for a high-performance processor with a reconfigurable data-path (RDP) using SFQ circuits, and show its feasibility and effectiveness.

II. HIGH-PERFORMANCE PROCESSOR WITH SFQ-RDP

The basic component of SFQ digital circuits is a superconducting loop with Josephson junctions. An SFQ, which appears as a voltage pulse, is used as the carrier of information. The width of an SFQ pulse is several pico-seconds and the height is about 1mV. The energy consumed for switching is much smaller than CMOS circuits. By the passive transmission line (PTL) technology developed recently, ballistic transmission of an SFQ pulse on superconducting wirings is possible.

We have proposed a high-performance processor with an RDP using SFQ circuits. An RDP consists of a lot of floating-point units (FPUs) and operand routing networks (ORNs) which connect the FPUs. We reconfigure the RDP to fit a computation, i.e., a group of floating-point operations, appears in a 'for' loop of numerical programs by setting the route in ORNs before the execution of the loop.

III. RESEARCH RESULTS

We have developed a Nb 9-layer 1μm fabrication process with a device structure having the active layers at the top, the PTL layers in the middle, and the DC power layers at the bottom [1]. To fabricate this structure, we have developed a higher quality planarization. We have fabricated shift registers for process evaluation, and confirmed the correct operation of four 2,560-bit shift registers having 10,281 junctions on a chip.

We have developed a logic cell library for this new fabrication process [2]. We have also developed CAD tools including a clock tree synthesizer and an automatic wire router.

We have demonstrated 112-GHz operation in a 4x4 SW. The area is reduced by more than 80% compared to that made with the conventional Nb 4-layer 2μm process. The device density of 1.8×10^6 JJs/cm^2 is the world's highest in SFQ LSIs.

We have developed an SFQ bit-serial half-precision FP-adder and FP-multiplier using the 2μm process [3]. They have operated at 20GHz and 32GHz, respectively. We have also designed and fabricated circuit components of an FPA and an FPM using the 1μm process. They have operated at about 80GHz.

As an SFQ-RDP prototype, we have developed small-scale RDPs with arithmetic units as a processing unit. A 2x3 SFQ-RDP fabricated using the 2μm process has operated at 23GHz [4]. This circuit with 14,040 Josephson junctions is the world's largest SFQ-LSI. A 2x2 SFQ-RDP has been also designed and fabricated using the 1μm process. It has operated at 45GHz with a power dissipation of 3.4mW. SFQ LSIs have distinct advantage to CMOS devices in energy-delay products.

We have determined the architectural specifications of an SFQ-RDP through a design process using data-flow-graphs (DFGs) of scientific application benchmarks. We have developed compiler tools for an SFQ-RDP system [5]. Reconfiguration bit-streams for an RDP are generated by the routing and mapping tools for DFGs extracted manually from critical segments of a target application. According to our estimation, the performance for two-dimensional heat application and that for FDTD application are 50.6 and 23.4GFLOPS, respectively, which are comparable to those of a system with GPUs reported in literature.

Through the research, we have shown that we can design and fabricate large scale SFQ circuits, that we will be able to realize an SFQ-RDP, and that a processor with an SFQ-RDP is effective.

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