Ultralow power TFT fabricated by use of nitric acid oxidation method

Hikaru Kobayashi
Institute of Scientific and Industrial Research, Osaka University, and CREST, Japan Science and Technology Agency
8-1 Mihogaoka, Ibaraki,
Osaka 567-0047, Japan

***Abstract*—We have developed a fabrication method of a gate oxide layer in TFTs by use of the nitric acid oxidation of Si (NAOS) method. Immersion of Si in nitric acid aqueous solutions forms an ultrathin (i.e., ~1.8 nm) SiO_2 layer with the low leakage current, and thus, the thickness of a gate oxide layer deposited by use of the CVD method can be decreased to ~20 nm. The TFTs with the ultrathin NAOS SiO_2/20 nm CVD SiO_2 stacked gate oxide structure can be operated at 1.5 V, indicating that the consumed power is decreased to 1/64 of that of conventional TFTs driven at 12 V.**

Keywords-ultralow power, TFT, thin gate oxide, NAOS

I. INTRODUCTION

Thin film transistors (TFTs) are fabricated on glass substrates, which makes high temperature processes such as thermal oxidation of Si unavailable. Therefore, a gate dielectric layer in TFTs is usually formed by deposition methods such as chemical vapor deposition (CVD). However, interfacial characteristics of a deposited layer are poor, e.g., high interface state density [1,2], because of contaminants present on the surface before deposition and incomplete interfacial chemical bond formation. Bulk properties of the deposited layer are also poor due to inclusion of undesirable species such as water, hydrocarbon, etc, and porous structure [3,4]. Consequently, a thick gate oxide layer in the range between 50 and 100 nm is required to achieve a sufficiently low gate leakage current. However, the thick gate oxide layer increases the driving voltage of TFTs, resulting in high power consumption. The thick gate oxide layer also makes miniaturization of TFTs difficult.

We have developed a low temperature formation method of SiO_2/Si structure by use of nitric acid (HNO_3) aqueous solutions, i.e., the nitric acid oxidation of Si (NAOS) method [5-7]. Immersion of Si in HNO_3 aqueous solutions with concentration higher than 68 wt% at temperatures lower than 120 °C can form an ultrathin (i.e., 1.2~1.8 nm) SiO_2 layer with the leakage current density lower than that of a thermally grown SiO_2 layer with the same thickness. In the present study, the NAOS method has been used to fabricate gate oxide in TFTs. Due to the excellent characteristics of the NAOS SiO_2 layer, the thickness of the CVD SiO_2 layer can be decreased to ~20 nm, resulting in a decrease in the TFT driving voltage to 1.5 V.

II. EPERIMENTS

A ~100 nm silicon nitride layer was deposited on glass substrates in order to prevent diffusion of contaminating species from glass. ~50 nm thick amorphous Si layer was deposited by use of plasma-enhanced CVD method, followed by laser annealing to crystallize. Then, the specimens were immersed in 68 wt% HNO_3 aqueous solutions at room temperature to form a NAOS SiO_2 layer. On the NAOS SiO_2 layer, ~20 nm thick SiO_2 layer was deposited by use of the plasma-enhanced CVD method, resulting in the ultrathin NAOS SiO_2/~20 nm CVD SiO_2 stacked gate oxide structure. Source and drain regions were defined by implantation of phosphorus ions, and gate electrodes were produced by deposition of a tungsten layer.

III. RESULTS AND DISCUSSION

Figure 1 shows the current-voltage curves for the NAOS SiO_2/Si(100) structure. The thickness of the SiO_2 layer estimated from the area intensity ratio between the SiO_2 Si 2p peak and the substrate Si 2p peak in the X-ray photoelectron spectra (cf. inset) was 1.8 nm. The leakage current density of the NAOS SiO_2 layer formed at room temperature was nearly the same as that of the thermal oxide layer grown at ~900°C [8].

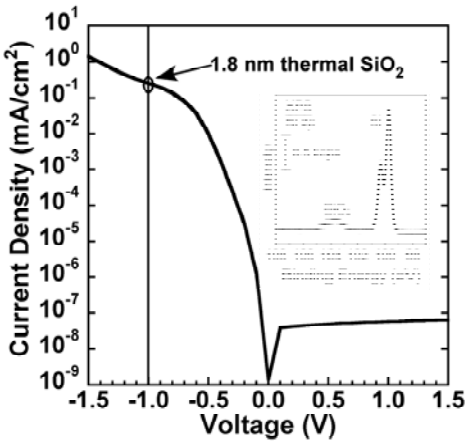

Fig. 1 Current-voltage curves for the <Al/1.8 nm NAOS SiO_2/Si(100)> structure with the NAOS SiO_2 formed at room temperature.

Figure 2 shows the drain current vs. source-drain voltage (I_d-V_{s-d}) characteristics of the TFTs with the ultrathin NAOS SiO_2/~20 nm CVD SiO_2 stacked gate oxide structure. It should be noted that the sub-micrometer (i.e., 0.9 μm) TFTs have been achieved because of the thin gate oxide thickness of ~20 nm. The I_d-V_{s-d} curves possess ideal feature with saturation. The drain currents for both the P-ch and N-ch TFTs are sufficiently high even at the driving voltage of 1.5 V, demonstrating that the TFTs work at 1.5 V. Because consumed power is proportional to the square of the driving voltage [9], the power consumption of the fabricated TFTs is 1/64 of that of conventional TFTs driven at 12 V. The threshold voltage of the P-ch and N-ch TFTs are −0.5 and 0.5 V, respectively. These low threshold voltages enable the 1.5 V TFT operation.

Figure 3 shows the drain current vs. the gate voltage curves for the TFTs with the ultrathin NAOS SiO_2/~20 nm CVD SiO_2 stacked gate oxide structure. The on-current is approximately 10^{-5} A while the off-current is 10^{-14}, leading to the high on/off ratio of 10^9. Such a high on/off ratio is attributable to the low off-current which is in turn due to the low leakage current characteristic of the NAOS SiO_2 layer, i.e., the NAOS SiO_2 layer effectively blocks the leakage current. In the sub-threshold region, the current increases rapidly with the gate voltage, and the sub-threshold swing (S) values for both the P-ch and N-ch TFTs are estimated to be ~80 mV/dec., i.e., close to the theoretical limit of 60 meV [10]. The low S-value demonstrates excellent interfacial properties of the NAOS SiO_2 layer with a low interface state density.

The channel mobility of the P-ch and N-ch TFTs are ~100 and ~200 cm^2/Vs, respectively, nearly independent on the channel length. This result indicates that the gate oxide layer does not degrade the channel mobility, and it is determined only by the poly-Si film. The high channel mobility also demonstrates the excellent characteristics of the NAOS SiO_2 layer.

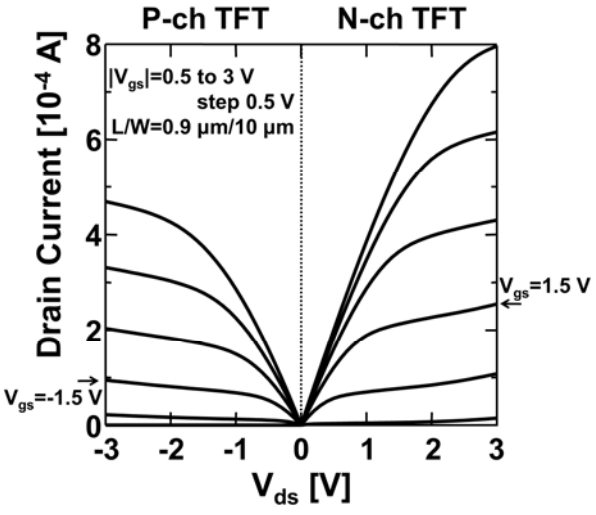

Fig. 2 Drain current vs. source-drain voltage curves for the P-ch and N-ch TFTs with the ultrathin NAOS SiO_2/~20 nm CVD SiO_2 stacked gate oxide structure.

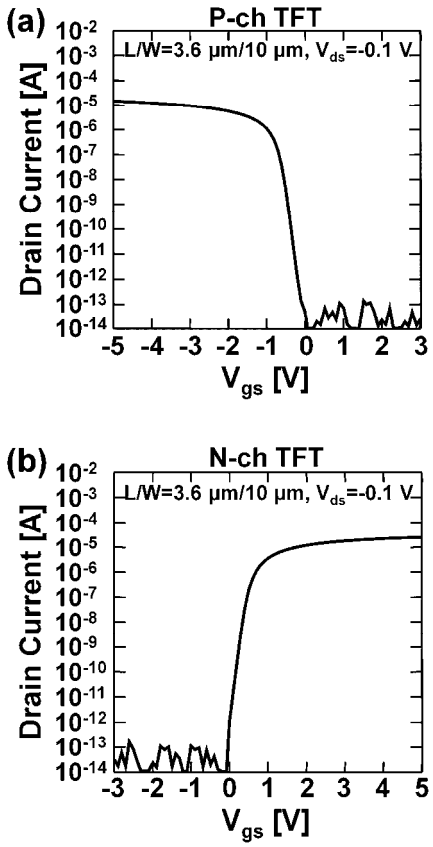

Fig. 3 Drain current vs. gate voltage curves for the P-ch (a) and N-ch (b) TFTs with the ultrathin NAOS SiO_2/~20 nm CVD SiO_2 stacked gate oxide structure.

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