

Development of Flex Power FPGA

A Novel FPGA Design with Power Reconfigurability

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Abstract—Vt-optimizable ultra low leakage power FPGA, called Flex Power FPGA, to solve the serious static power consumption problem in FPGA, and its test chips and CAD tools development supported by CREST ULP grant, are presented.

Keywords - FPGA; static leakage power reduction; Vt optimization

I. INTRODUCTION

Because of increasing NRE cost for LSI development, and increasing demand for high-mix low-volume production, FPGA has evolved to an indispensable standard LSI component of wide range of ICT products.

Static leakage power consumption has been one of the most challenging issues in semiconductor industries for the last 10+ years. Especially, static power consumption in FPGA is serious problem, because FPGA uses far more transistors per unit logical function. Vt optimization based on critical path analysis of the circuit has become a very popular technique to reduce leakage power, however this technique cannot be applied to FPGA, because you cannot determine which logic block should be low-Vt or high-Vt at chip manufacturing stage.

II. FLEX POWER FPGA

We proposed a Vt-optimizable ultra low leakage power FPGA, called Flex Power FPGA. Electrical Vt control technique, such as body biasing, is applied to design a power configurable logic block and switch block, and newly introduced *power configuration registers* control the speed and power consumption trade-off based on the analysis of the configured circuit. As a result, Flex Power FPGA provides *power configurability* as well as circuit configurability.

Preliminary evaluation using 20 MCNC benchmark circuits shows that Flex Power FPGA can reduce its static power by up to 1/30 without changing its operating speed.

III. CREST ULP DEVELOPMENTS

We have started our Flex Power FPGA development plan as a CREST ULP project to demonstrate the potential of the Flex Power FPGA concept.

Several generations of prototype Flex Power FPGA test chips have been developed for empirical study on power reduction, speed improvement and area overhead with real design.

The latest test chip (1002 chip) contains 6 by 6 basic FPGA tiles, and each tile consists of a clustered logic block with 2 basic logic elements, and a switching block with 2 unidirectional wire segments of length 2 per direction. Each basic tile is divided into 16 separate Vt control domains, and total number of VCDs of the chip is 576.

CAD tool is the other important side of FPGA developments. Practically usable Flex Power FPGA CAD tool flow, including dedicated automatic Vt mapping tool for static power reduction, has been developed as another part of CREST ULP developments. Our tools successfully configure the test chips described above, as well as the correctness of the tools is strictly verified by a formal verification tool using circuit designs of practical size such as 16 bit microprocessor.

Measurement results show that the latest test chips configured by our CAD tool achieves substantial leakage reduction of 1/4.8 using our proposed method at this moment, although the Vt controllability of the MOS device provided by the fab. mainly limits the reduction ratio. Detailed analysis of the test chip also suggests further improvement possibilities, including more balanced Vt control domain granularity design, and full chip FPGA implementation for evaluation with more complex and realistic benchmark circuits. New improved test chip is under development, and will be taped out very soon.

These results of CREST ULP developments have already kicked off the evolution of FPGA into several dimensions. Test chip design and CAD tools have been transferred to other research projects, including advanced SOI implementation for further leakage reduction with less area penalty, as well as extended 3D implementation of the chip.

IV. CONCLUSIONS

We proposed a Vt-optimizable ultra low leakage power FPGA, called Flex Power FPGA, to solve the serious static power consumption problem in FPGA. Several generations of prototype test chips and practically usable CAD tool flow, including dedicated automatic Vt mapping tool for static power reduction, have been developed supported by CREST ULP grant. Measurement results show that the latest Flex Power FPGA test chips configured by our CAD tool achieves substantial leakage reduction of 1/4.8. Our test chip design and CAD tools are transferred to other research projects as well.