ULP-DDNS

# *Ultra-Low-Power Data-Driven Networking System*

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ULP-DDNS

# Outline

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  - Traffic Reduction Schemes of Ad Hoc Network
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  - Power Control Schemes in Self-Timed VLSI Realization
- ULP-DDNS Prototype and Power Simulator/Validator
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- Current Status and Future Directions

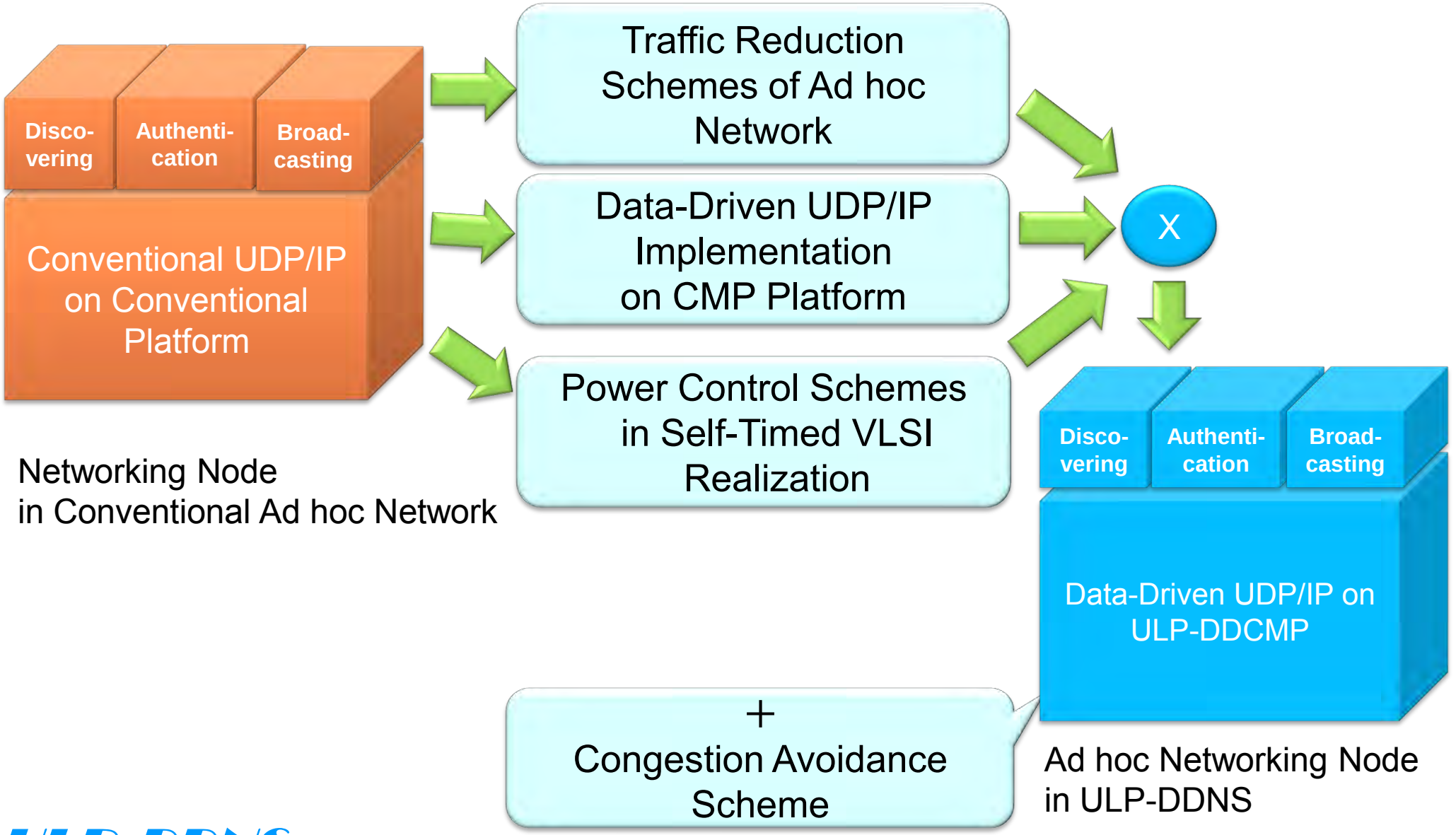
# Objective and Our Solution

- Objective

  Sustaining communication capability through sufficient time by reducing power consumption in networking system, especially in emergency.

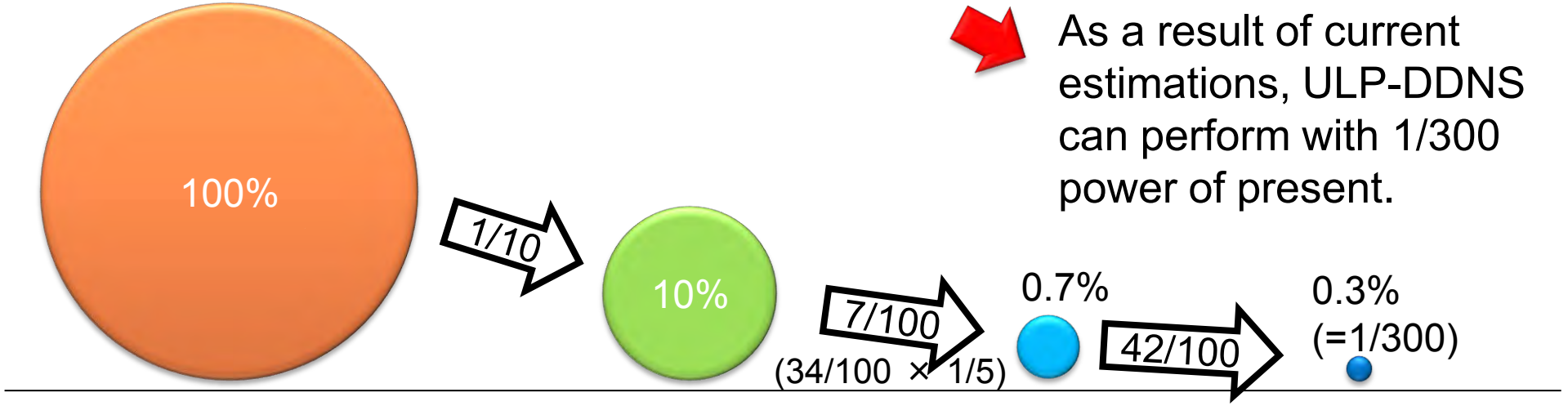
- ULP-DDNS
  - can provide longer lifetime or stronger dependability under severe power budget and traffic condition.
    - Each networking node only consumes the minimum and essential power without any runtime overhead.
  - ultimately utilizes passive data-driven principle throughout ad hoc networking scheme, CMP platform dedicated to multiple UDP/IP processing and its self-timed VLSI realization.

# Scenario to Ultra-Low-Power Consumption



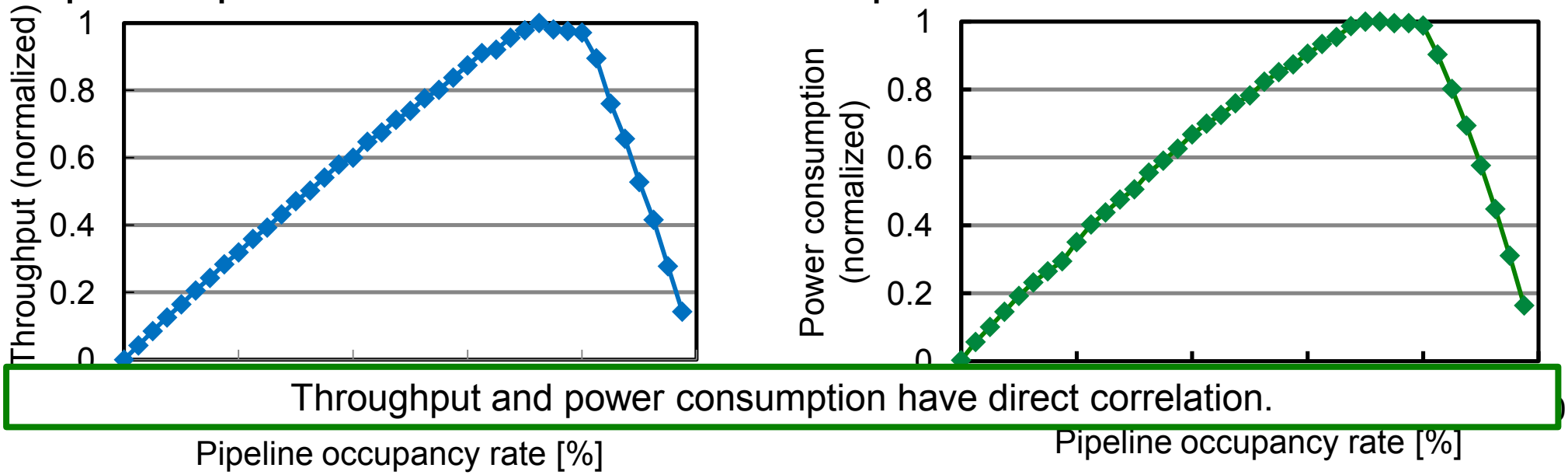
# Total Power Reduction in ULP-DDNS (Current Status)

- Power reduction effect of each scheme is independent and can be multiplied with the others.
  - Traffic reduction schemes reduce 90% power consumption of present.
  - Data-driven UDP/IP Implementation on CMP platform reduces 93% power consumption of present.
  - Power control schemes in self-timed VLSI realization reduces 58% power consumption of conventional network processor (e.g. XScale).



# Data-Driven Scheme without Redundant Power Consumption

- Data-driven scheme;
  - has passive operation mode to naturally realize communication processing.
  - realizes multiprocessing without any context switching overhead.
- To keep above features, self-timed pipeline was adopted as power-performance-efficient VLSI implementation.




Throughput and Power Consumption in Self-Timed Circular Pipeline

This feature is expected to naturally save redundant power consumption.

# ULP Schemes Based on Data-Driven Principle

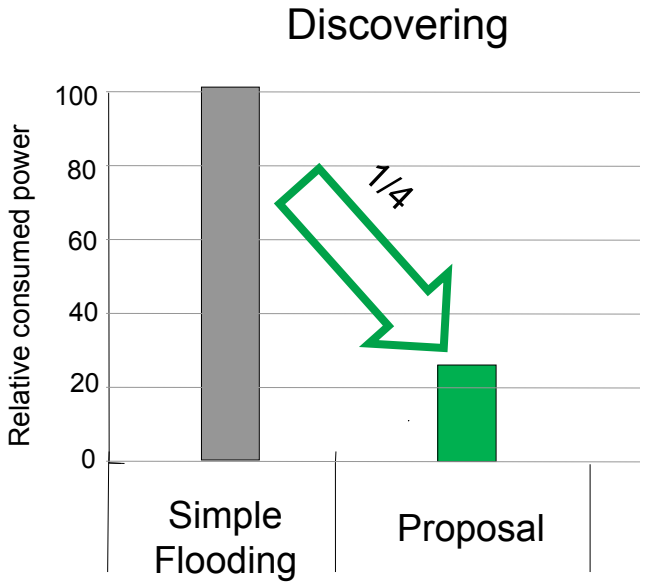
- Traffic reduction schemes of ad hoc network
  - Efficient discovering, authentication, broadcasting
- Data-driven UDP/IP implementation on CMP platform
  - Concurrent execution of header processing and datagram manipulation
  - Optimized circular instruction execution pipeline in CMP core: ULP-CUE
  - Core-level power gating and DVS *(conventional scheme)*
  - Intra-stage power gating *(conventional scheme)*
- Power Control Schemes in Self-timed VLSI realization
  - Self-timed power-aware pipeline
    - Stage-by-stage power gating
    - DVS by PID control

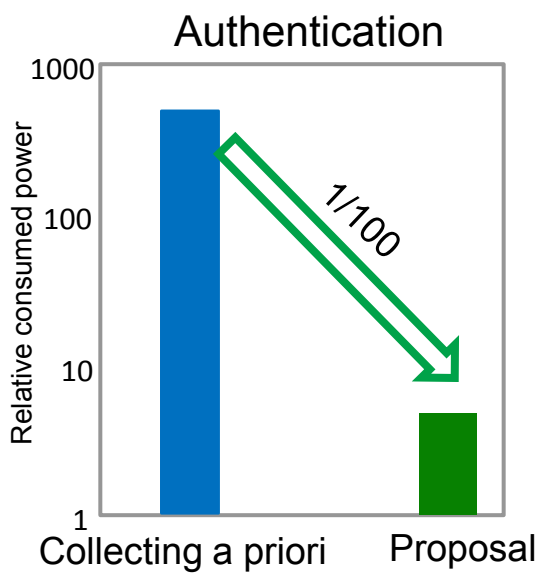
# Two phases of Ad hoc Network for Emergency

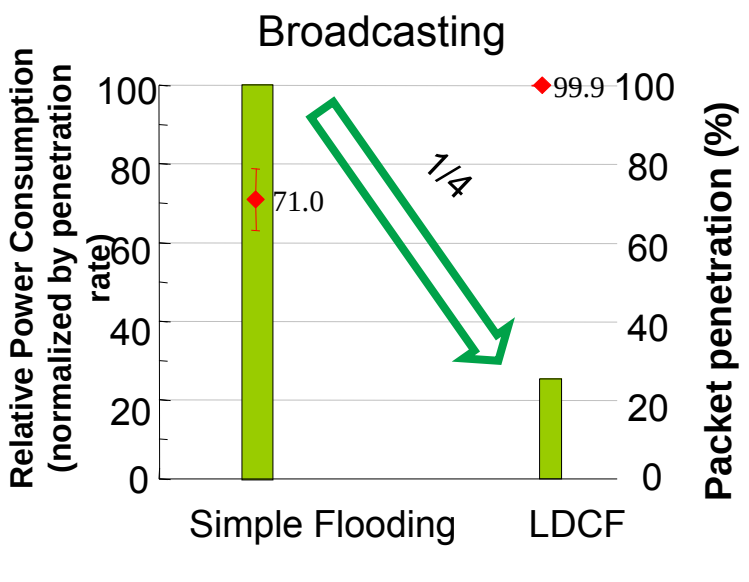
- Just after emergent situation happens, two phases are possible and following 3 functions are needed.
  - Phase 1: Transient phase (unspecified communication)
    - Little information about other nodes are given so that unicast/multicast communication is very difficult
    - Discovering necessary information by a person over the network such as shelter, hospital, etc. is indispensable function in this phase (pull type communication with unspecified peer)
    - Broadcasting useful and urgent information all over the network is also indispensable function in this phase (push type communication to all the unspecified peers)
  - Phase 2: Stable phase
    - Authentication of public key is needed for communication with specified peers with cyphered message
    - Broadcasting is also useful in this phase

# Traffic reduction of Ad hoc Network (10%)

- Most energy consuming function is packet transmission and reception so that reduction of number of packets is the most efficient.
  - Discovering: Narrowing the search area using GPS
  - Authentication: Collection of necessary certificates only
  - Broadcasting: Eliminating rebroadcast by monitoring local load condition




Estimation based on a typical traffic ratio shows 10% power consumption of conventional network.

# Data-Driven Implementation of UDP/IP (34%)

- Realizes UDP/IP handling in Ultra-Low-Power Consumption
  - Shorter TAT reduces power consumption by fully utilizing power control scheme on platform and VLSI realization
    - Header/Data handling in UDP/IP is concurrently realized to shorten TAT.
    - Instruction set architecture is optimized for UDP/IP handling.
- Concurrent execution of header handling and datagram manipulation
  - TAT is reduced to 50%～84% by the concurrent execution.
- Instruction set architecture for UDP/IP
  - TAT is reduced to 67% by utilizing instruction set in UDP/IP handling.

TAT: Turn-Around Time

The implementation reduces the power consumption to 34%～56%

# Evaluation on Power Reduction by ULP-CUE (20%)

- Feasibility Study: Power Consumption in UDP/IP handling on Previous Version of Data-Driven Processor

  ※Previous Version: a hybrid architecture by data-driven and control-driven schemes

  - Pipeline tact is 15% of the frequency in conventional NPU. (≒ Power Consumption is low)
  - Data-driven implementation of protocol Handling
    - reduces power consumption to 40% in conventional NPU.
- Tuning in Circuit Area for Ad hoc Networking Oriented
  - The number of the entries of Matching Memory is reduced to one-half.（64→32）
  - Elimination of the non-data-driven circuit parts
    - reduces power consumption to 50% in previous version of data-driven processor.

ULP-CUE: Ultra-Low-Power Coordinating Users' requirement and Engineering constraints
NPU : Network Processing Unit

CMP core, named ULP-CUE, reduces the power to 20%(=40%×50%) in conventional NPU.

# Self-Timed VLSI Realization

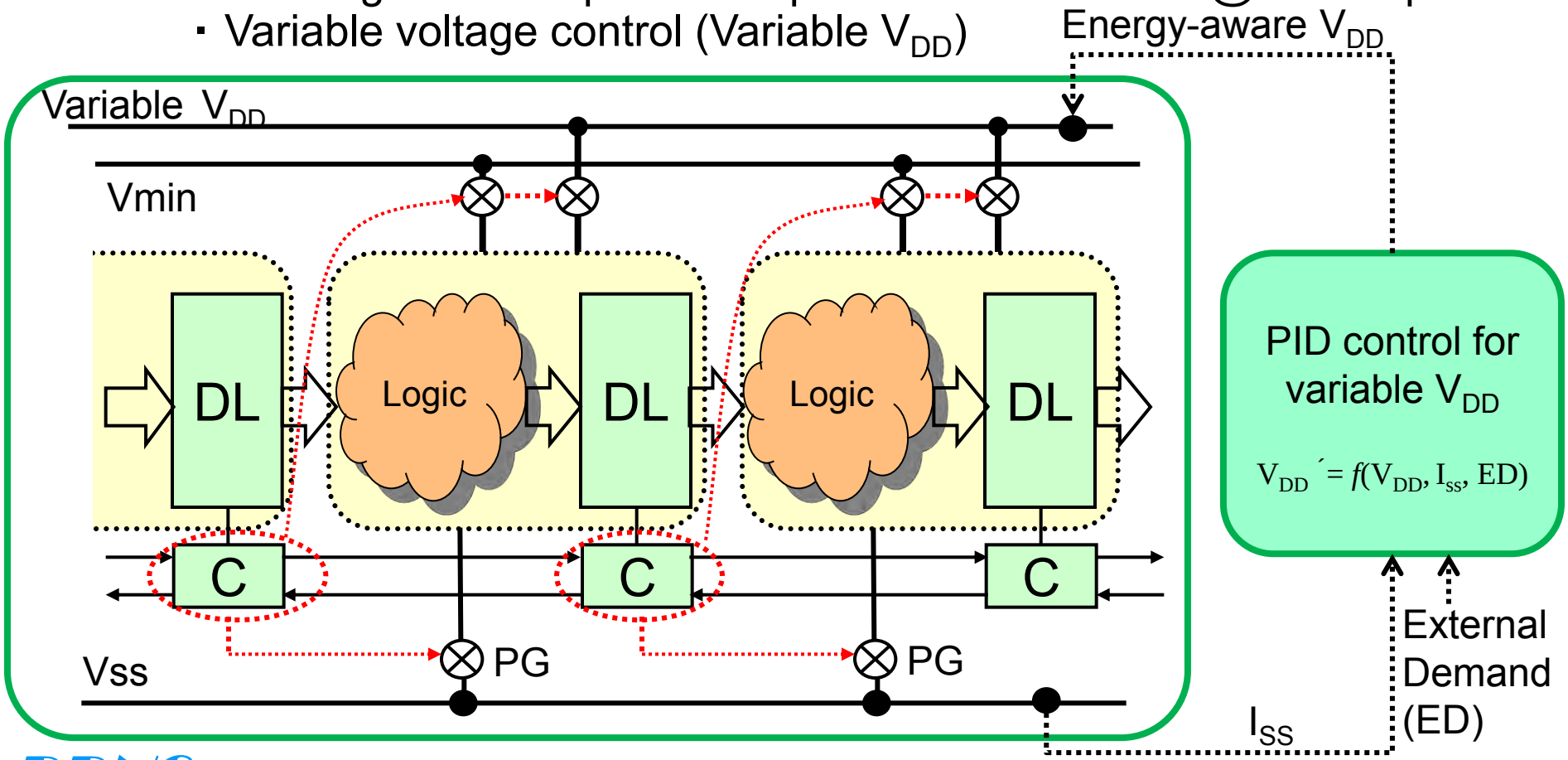
☆Self-timed power-aware pipeline with autonomous and localized power-control

Point 1: Cutting leakage power @ Idle phase

- Power gating (PG) / Vmin

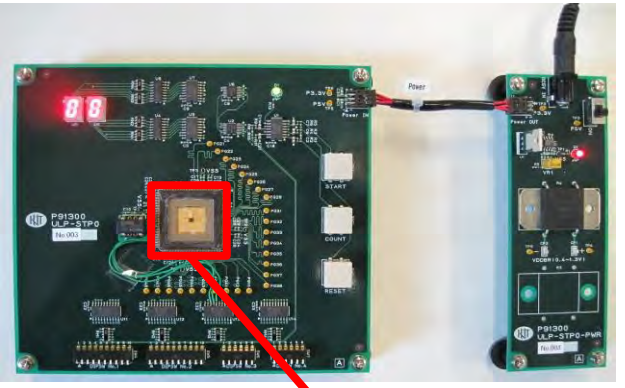
Point 2: Consuming essential power adaptive to dataflow rate @ active phase

- Variable voltage control (Variable $V_{DD}$)

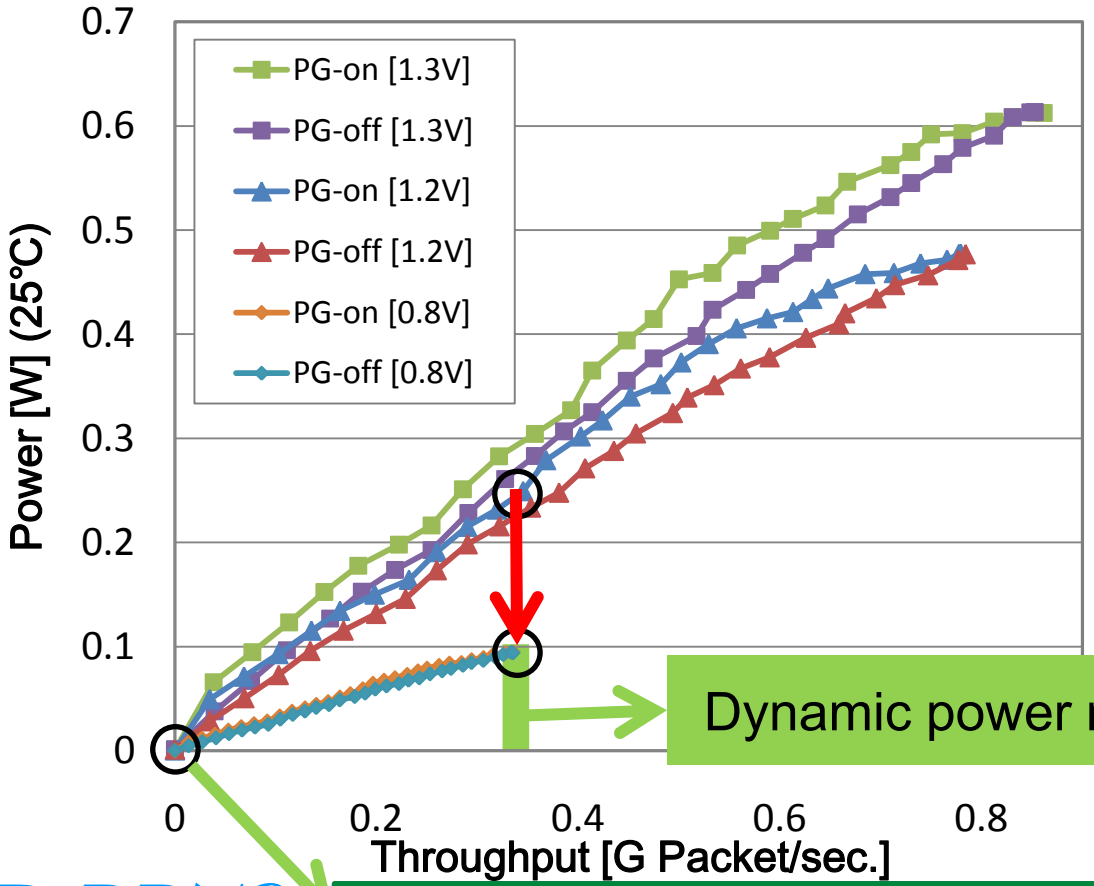


# Power Consumption on Self-Timed Power-Aware Pipeline (42%)

- Specification of 65nm CMOS 7ML experimental chip
  - 40-stage circular pipeline
  - 198 bit data path
  - Gray code encoder realized in every stage



Experimental chip of self-timed power-aware pipeline




Low power features
- no clock distribution power
- power ∝ throughput
- throughput ∝ supply voltage

Essential power consumption

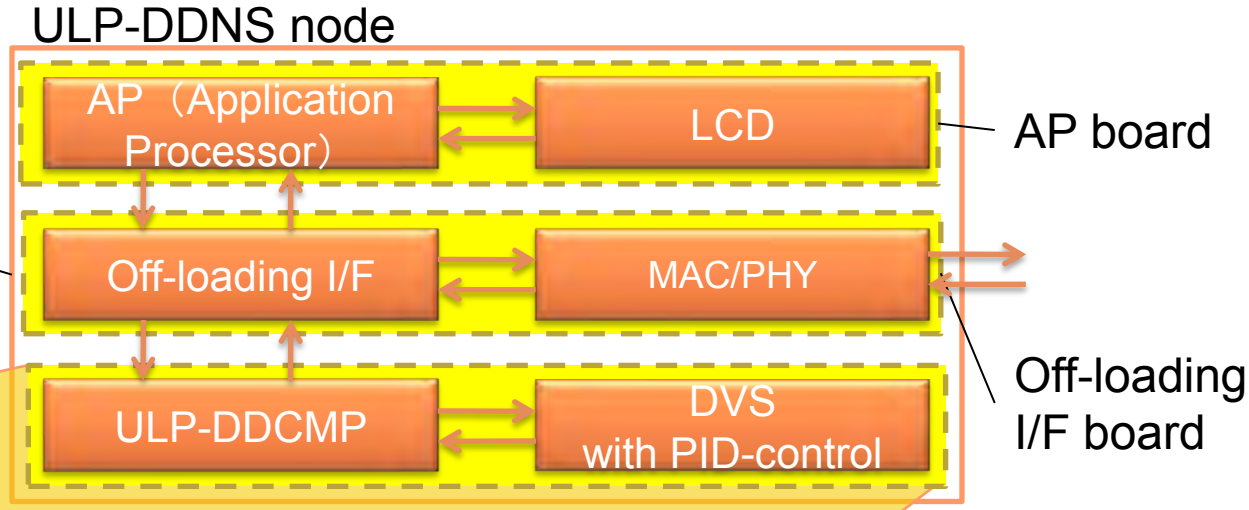
Dynamic power reduced to 42%

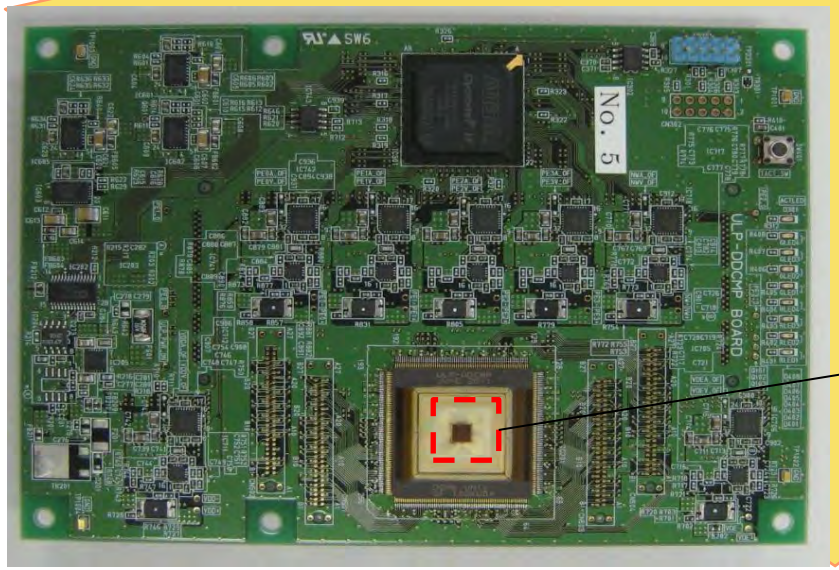
1.3V: Maximum
1.2V: Standard
0.8V: Minimum

leakage power reduction ⇒ 93% (1.23mW ⇒ 84μW)

# Prototype of ULP-DDNS Node

- ULP-DDNS node (under development)

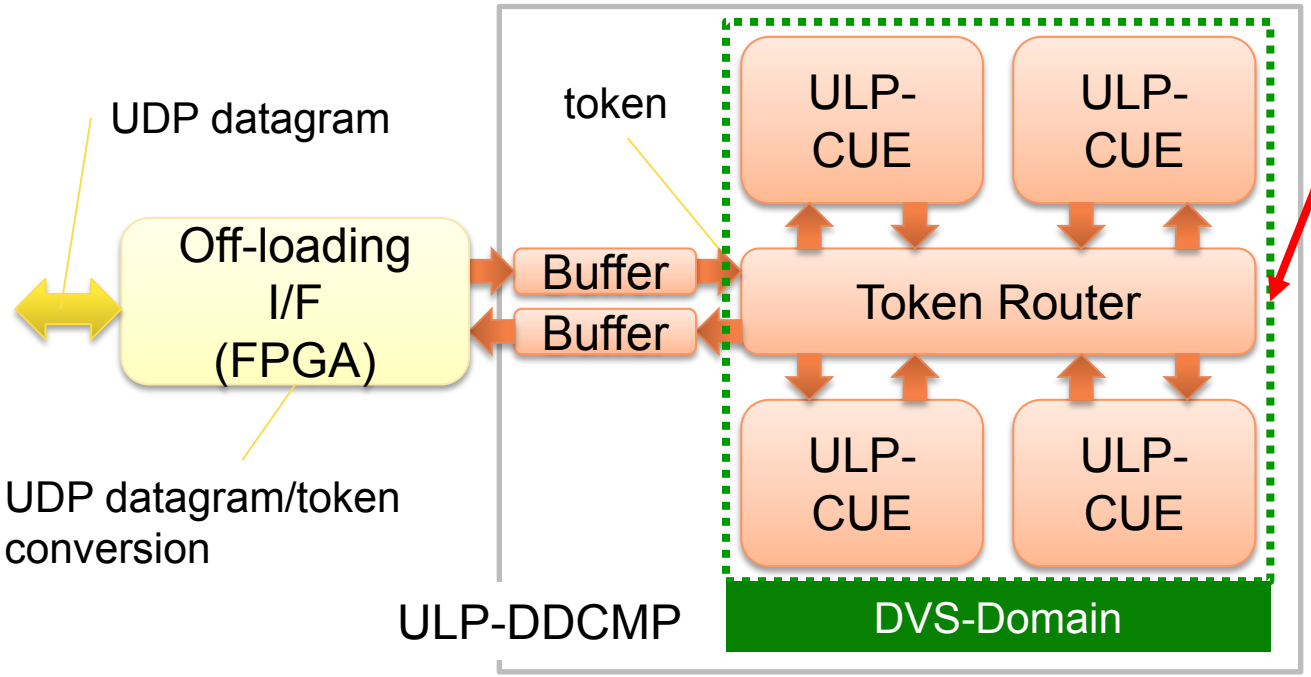

ULP-DDCMP board

ULP-DDCMP (ULP data-driven CMP) chip

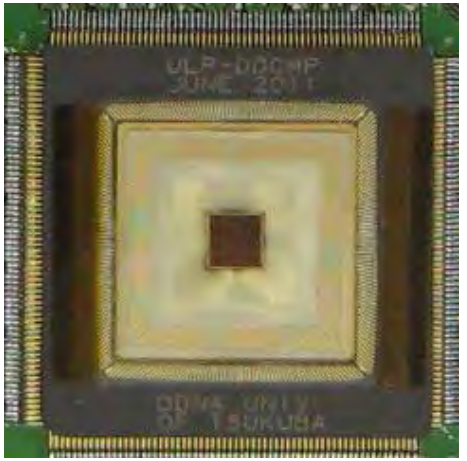
☆Specification of the prototype chip

- 65nm CMOS 7ML process
- Cores: 32-bit ULP-CUE x 4
- Die size: 4.2mm x 4.2mm

# Prototype LSI Chip (ULP-DDCMP)
# (fabricated in 2011/6)




☆PID control is realized on ULP-DDCMP board.

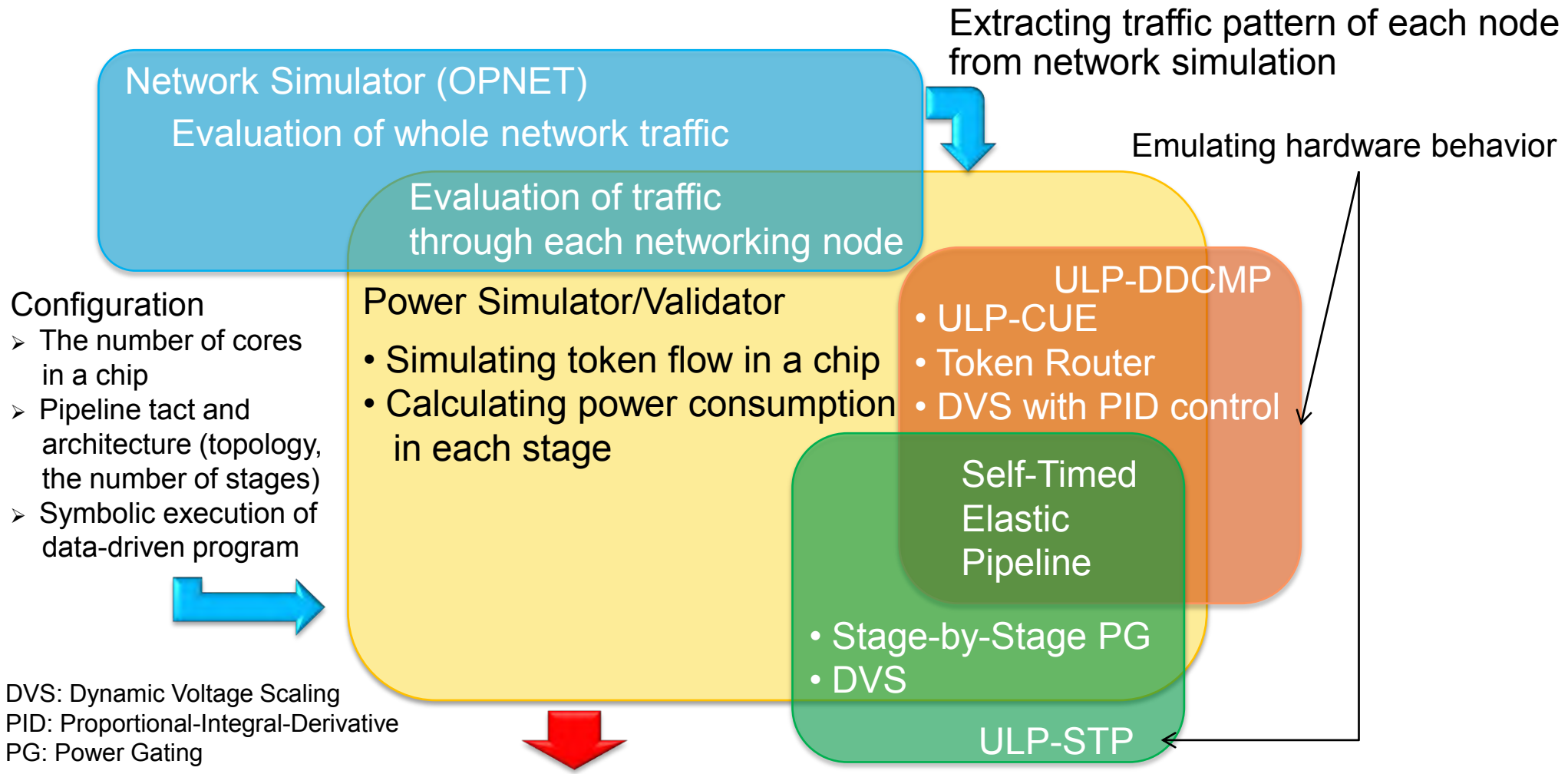


ULP-DDCMP in package

- ULP-DDCMP (Ultra-Low-Power Data-Driven CMP)
  - The simulation parameters for power simulator/validator are verified experimentally.

# Power Simulator/Validator for ULP-DDNS

- To validate power consumption reduced by our schemes



# Further Study of ULP-DDNS

- The next target is to reduce much more power.
  - The rescue rate at the disaster can be improved drastically if the lifetime of the networking node becomes several days from several hours.

- To Realize the target by fully utilizing fine-grained power gating scheme and DVS based on PID with minimum runtime overheads
  - Off-loading not only UDP/IP but also lower layer (MAC/PHY) and upper layer (Application)
  - Congestion/overload avoidance scheme

# Current Status and Future Directions

- ULP-DDNS

  can perform with 1/300 power of present by:

  - traffic reduction schemes of ad hoc network,
  - data-driven UDP/IP implementation on CMP platform and
  - power control schemes in self-timed VLSI realization

- Further Power Reduction to drastically improve the rescue rate

  should be realized by:

  - Off-loading not only UDP/IP but also lower layer (MAC/PHY) and upper layer (Application) and
  - Variable throughput based on DVS with PID-control