FY2013

Three-Dimensional Integrated Circuits Technology Based on Vertical BC-MOSFETs and Its Advanced Application Exploration

From planar to vertical – Create innovation through transistor evolution

As functions of electronic devices such as smartphones become increasingly sophisticated, short battery lifetimes are becoming a problem. Transistors are the key technology to drastically reducing power consumption. However, improvements in the commercialized planar type transistors are approaching their performance limit. With planar transistors, as the transistors become smaller, current control between electrodes becomes harder, and induces current leakage.

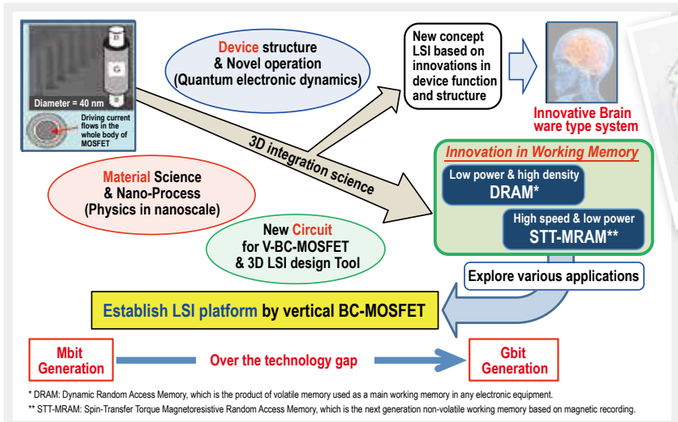
Hence, we have developed a totally new vertical transistor, a Vertical Body-Channel MOSFET, achieving a 1/100 to 1/1000 reduction in current leakage compared to standard planar transistors and a reduction in chip size at the same time. In addition, we succeeded in operating a 1-Mbit memory based on vertical transistors for the first time in the world.

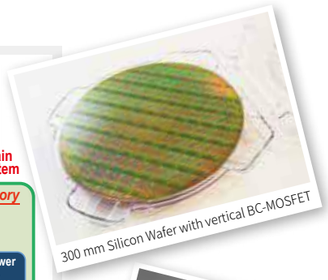
Accelerate the development of both integrated circuits and a range of electronic devices through the use of vertical transistors

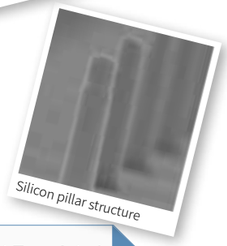
In the ACCEL project, we are developing a high-speed, large-capacity, and low-power-consumption working memory* by optimal utilization of vertical transistors. Fundamental common technologies will be strategically built to allow applications that can cover various integrated circuits.

And, by promoting the development and construction of the technology, we will create a new technological platform for semiconductor integrated circuits and lead the way for innovative power-saving integrated circuits. This will create new electronics systems that, for example, will improve smartphone performance 100 times over conventional ones and eliminate the need of charging for up to as long as month or more, contributing to an information-oriented, energy-saving, and ubiquitous society.

* A memory system that temporarily stores all system data from smartphones to supercomputers.




300 mm Silicon Wafer with vertical BC-MOSFET


Silicon pillar structure

Vertical Body Channel (BC-) MOSFET (Metal-Oxide-Semiconductor-Field-Effect-Transistor)

A vertical BC-MOSFET has a structure where a gate electrode surrounds a silicon pillar several dozen nanometers in diameter and source/drain electrodes are installed at the top and bottom. This allows the overall pillar to become a channel for electricity, suppressing leakage current and operating at voltages lower than previously.

Research Director

Tetsuo Endoh

Director of Center for Innovative Integrated Electronic Systems, and Professor of Graduate School of Engineering, Tohoku University

I have long felt that leakage current would become a critical issue for the development and dissemination of information terminals. Currently, planar transistors are faced with the challenge of increased power consumption along with miniaturization. Filled with a strong desire to change the device structure itself, I have been moving ahead with research on improving performance through 3D integration. I came up with the idea of *body channel type operation* to make the electric current directly flow through a silicon pillar. This idea went completely against the grain of the orthodox view that transistors should be planes.

In the ACCEL project, we will further improve the performance of our vertical transistor to develop a large-capacity, high-speed, and low-power working memory and eventually a logic LSI. The semiconductor field has grown impressively and steadily to this point, and is a critical industry in its influence on social paradigms. In particular, further improvement of its performance in capacity, speed, and power consumption is expected to create a range of large markets such as IoT and AI. As a result, Japan must continue R&D on semiconductors as a core technology.

I have come this far by clarifying new physical phenomena in nano-science one by one; developing integrated electronics technology step by step.

Program Manager

Toru Masaoka

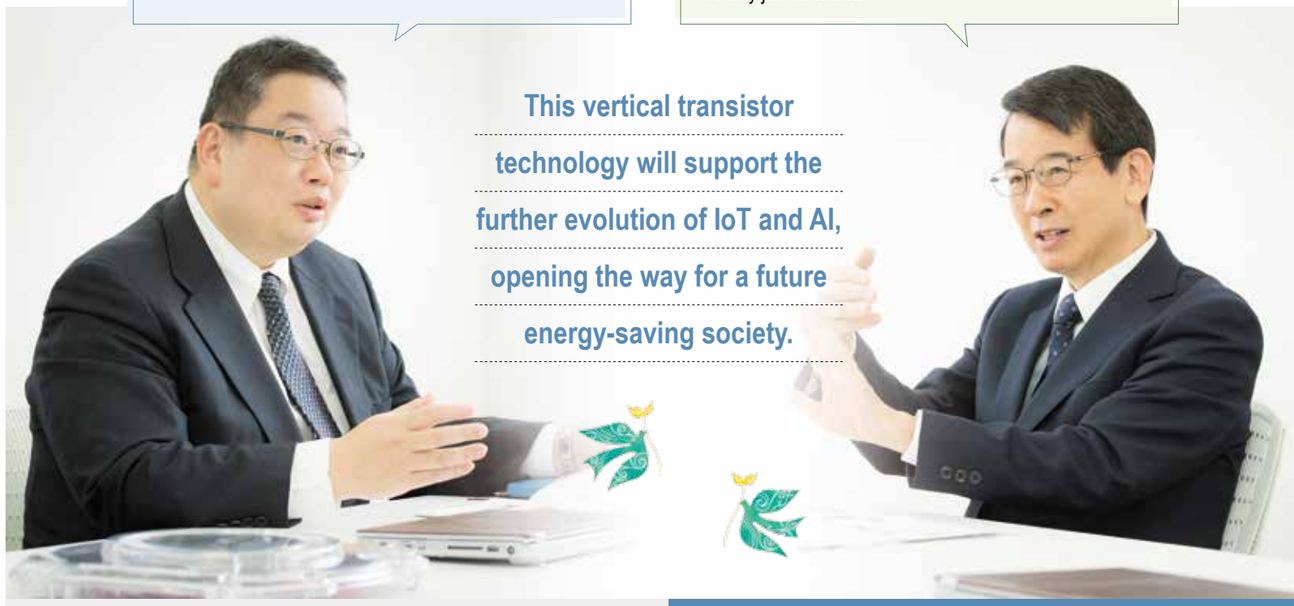
ACCEL Program Manager, Japan Science and Technology Agency

Since the potential of the vertical transistor was shown, 3D structure is becoming a mainstream part of next-generation integrated circuit development. My role is to promote R&D ahead of the world's top companies, laying the groundwork for its industrial application.

In the ACCEL project, I visit user companies and carry out other activities to spread the effectiveness of vertical transistors. At present, in addition to realizing working memory, we have started the development of fundamental technology with the aim of applying it to logic LSI. We have also clearly demonstrated that our vertical transistor can help reduce both the cell area and the amount of leak current, which are both urgent issues in logic LSI.

Practical implementation of this technology will bring innovation to the semiconductor industry and have a major influence on society in terms of information management, infrastructure, and so on. I would like to deepen our links with companies and contribute to the practical application of the vertical transistor.

The vertical transistor was greeted with astonishment by researchers all over the world. So for my next step, I would like to create industrial applications that astonish society just as much.



This vertical transistor technology will support the further evolution of IoT and AI, opening the way for a future energy-saving society.

PROFILE TETSUO ENDOH

1987: Graduated from the Department of Physics, School of Science, The University of Tokyo. Joined Toshiba Corporation; 1995: started work at Tohoku University; 2008: Professor, Research Institute of Electrical Communication, Tohoku University; in current post since 2012. R&D on integrated circuits, non-volatile memory/logic, and power electronics. Ph.D. (Engineering)

PROFILE TORU MASAOKA

1974: M.S. (Engineering), Keio University. Joined Toshiba Corporation; worked for Iwate Toshiba Electronics (currently Japan Semiconductor Corporation) and GlobalWafers Japan Co., Ltd. R&D on system LSI, and planning the commercialization of cutting-edge semiconductor technology.