On the control of GeO_2/Ge and metal/Ge interfaces toward metal source/drain Ge CMOS

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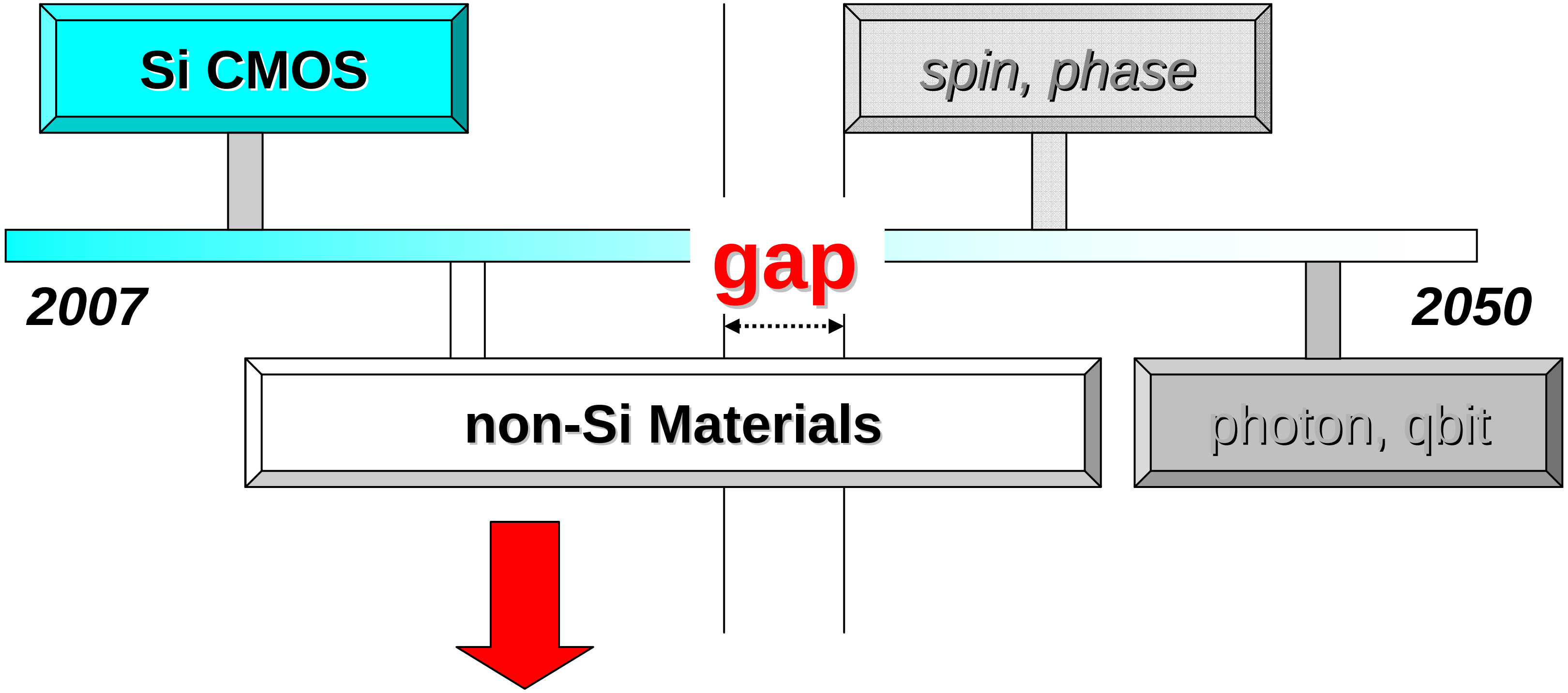
New things are not always healthy.



What is a promising candidate for non-Si Materials?
We have to take account of not only channel but also contact.

What is the Problem in Si ?

Si Microelectronics Research will end in 2015.

Si microelectronics is in the metabolic syndrome

Requirements for something new in the next step

Material should be simple.
Operation principle should be simple.
Process should be simple.

Outline

1. Background and Objective

Why Ge now ?

2. Ge MIS

GeO desorption

Ge/GeO_2 MIS Capacitors

3. Ge Schottky

Fermi-level Pinning

Ohmic contact to n-Ge

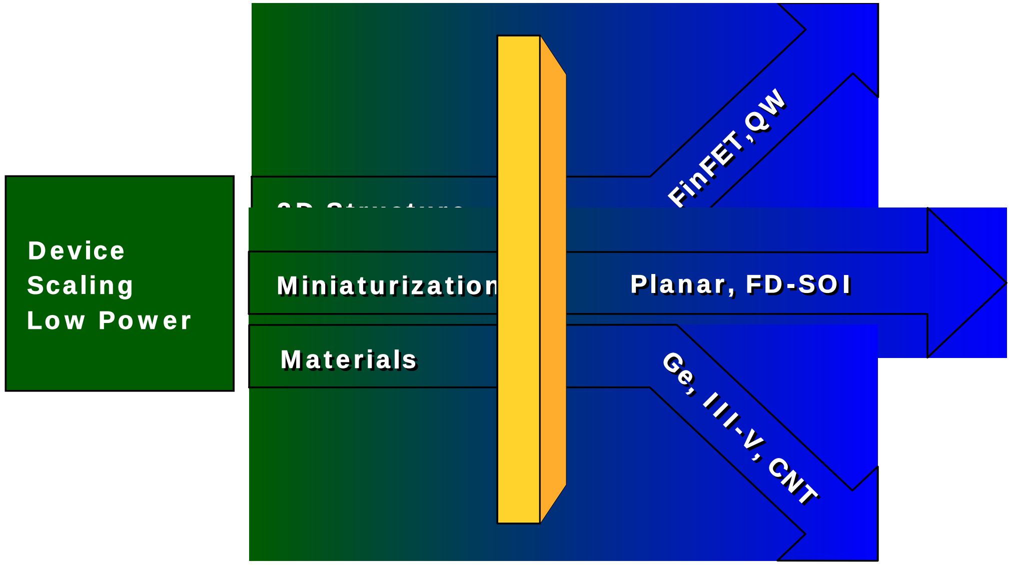
4. Ge-CMOS

p-MOSFET

n-MOSFET

5. Conclusions

Electron Devices in the Next Step



Device Scaling Low Power

3D Structure

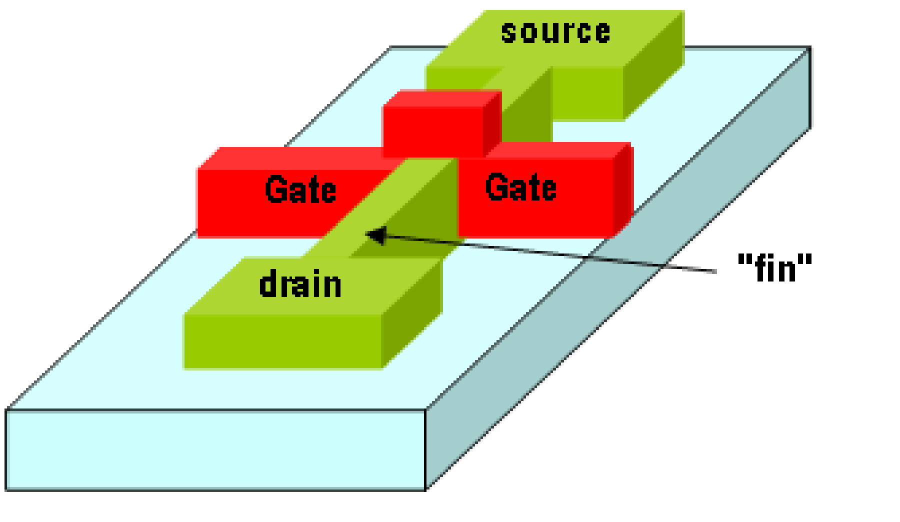
Miniaturization

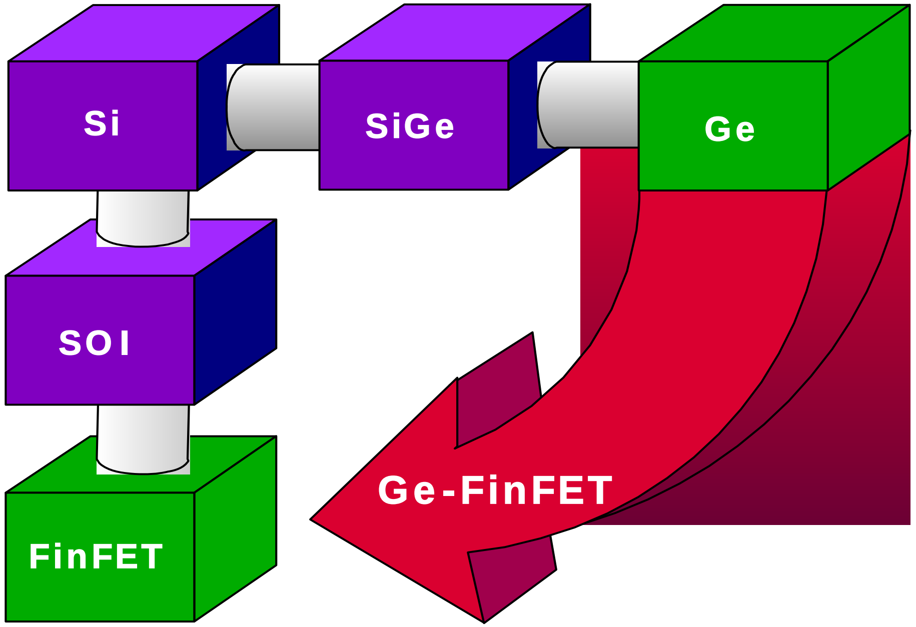
Materials

FinFET, QW

Planar, FD-SOI

Ge, III-V, CNT





Si

SiGe

Ge

SOI

FinFET

Ge-FinFET

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Demand for High Quality GeO_2/Ge Interface

High-k / Si

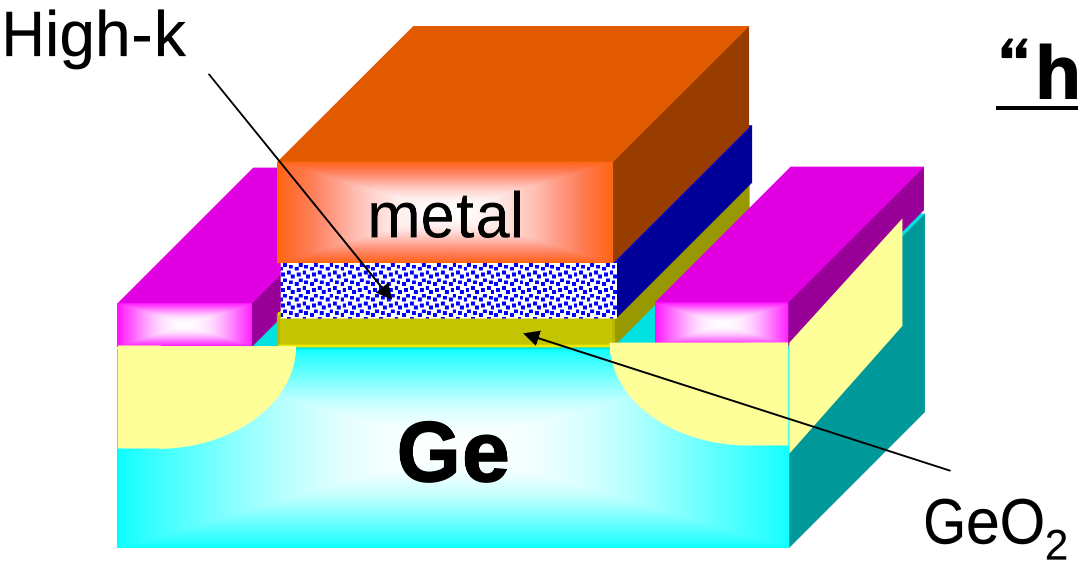
SiO_2 interface layer is inevitable for good device characteristics.

High-k / Ge

An appropriate High-k ?

GeO_2/Ge is thermodynamically unstable.

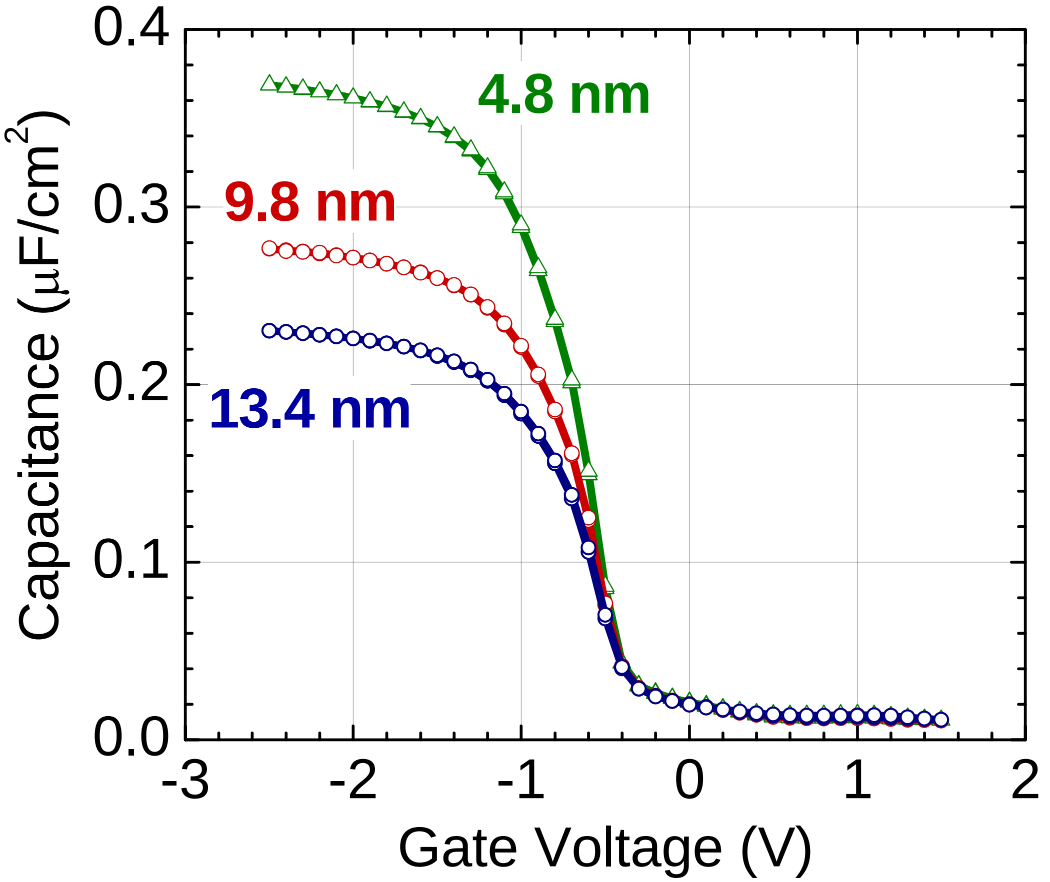
"high-quality" GeO_2 / Ge ?

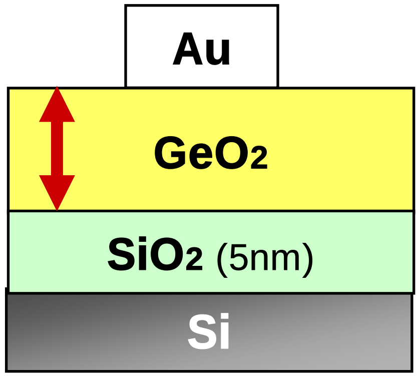


K. Kita et al., APL 85 (2004)

C-V Characteristics of $GeO_2/SiO_2/Si$ MIS

GeO_2 / SiO_2 / Si (<u>N_2 annealing at 600°C</u>)

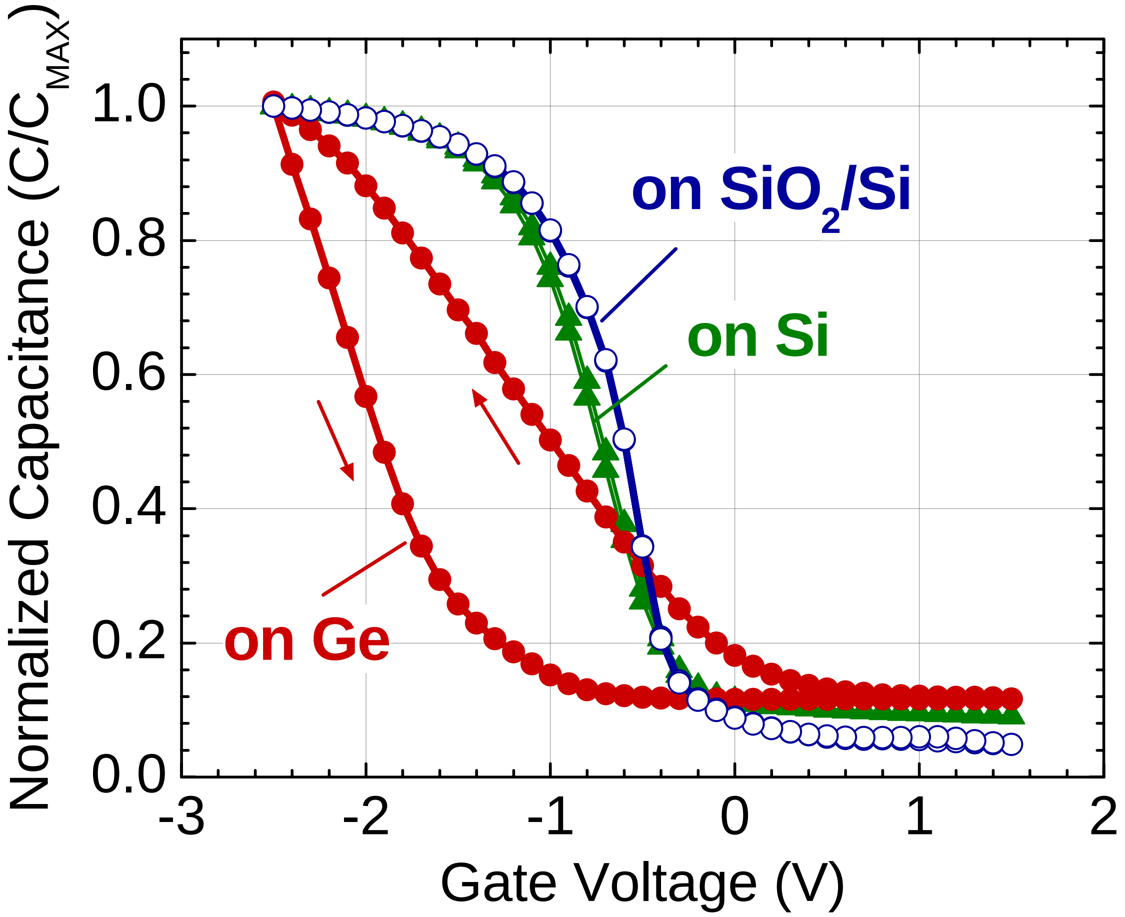




H. Nomura et al., IWDTF 2007

C-V Characteristics of GeO_2 MIS Capacitors

10nm-thick sputtered GeO_2 after **N₂ annealing at 600ºC**



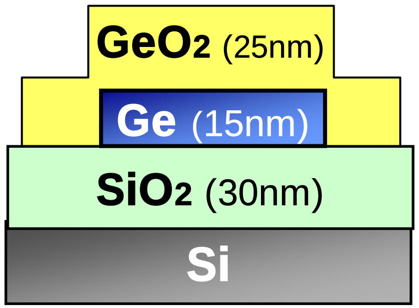
freq.=1MHz

K. Kita et al., ECS Trans. 3 (2007)

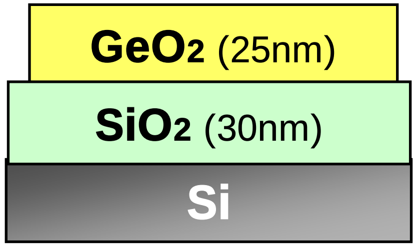
Evidence of GeO Volatilization from GeO_2/Ge

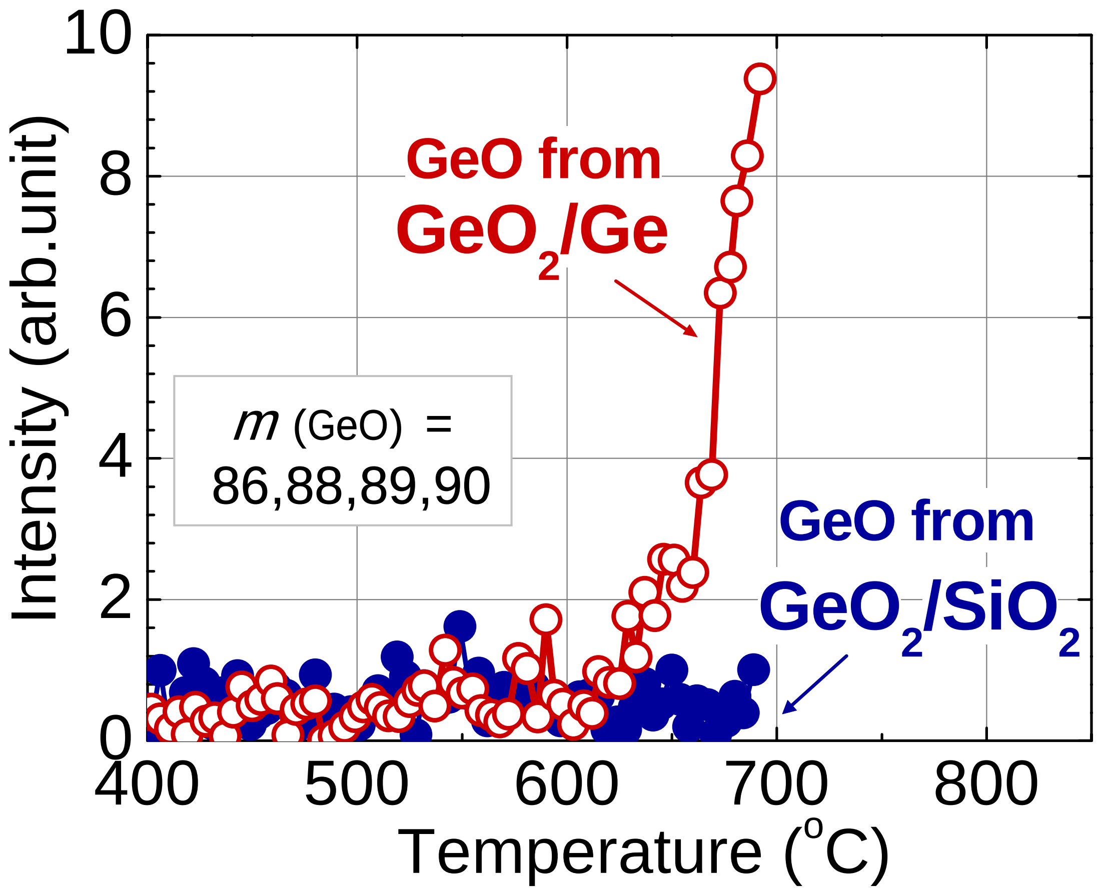
Thermal desorption spectroscopy（TDS）

GeO_2 / Ge



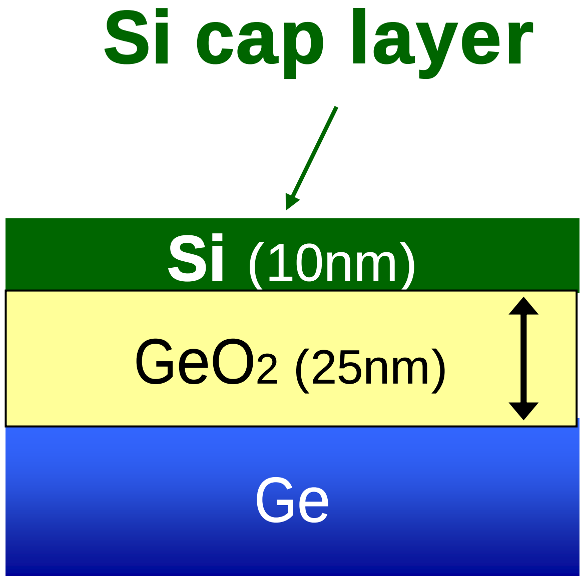
GeO_2 / SiO_2



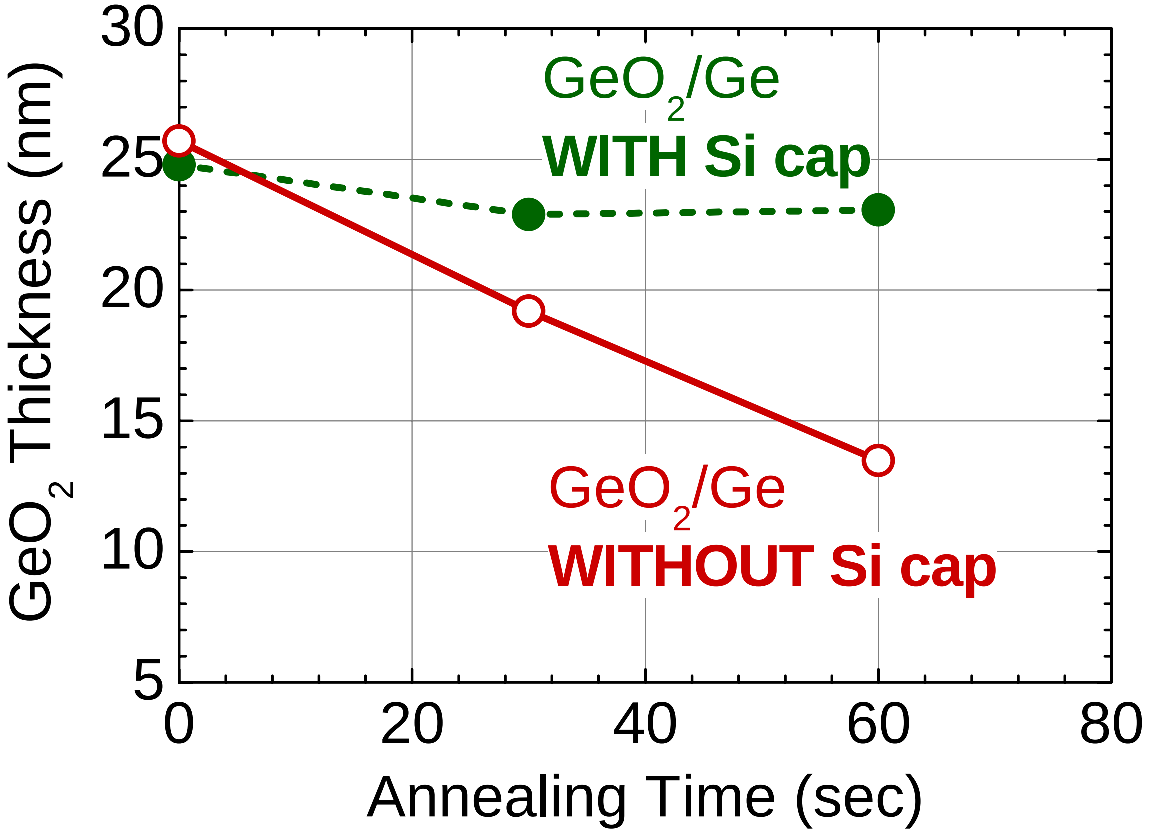


S. Suzuki et al., SSDM 2007

Suppression of GeO Desorption by Si Capping



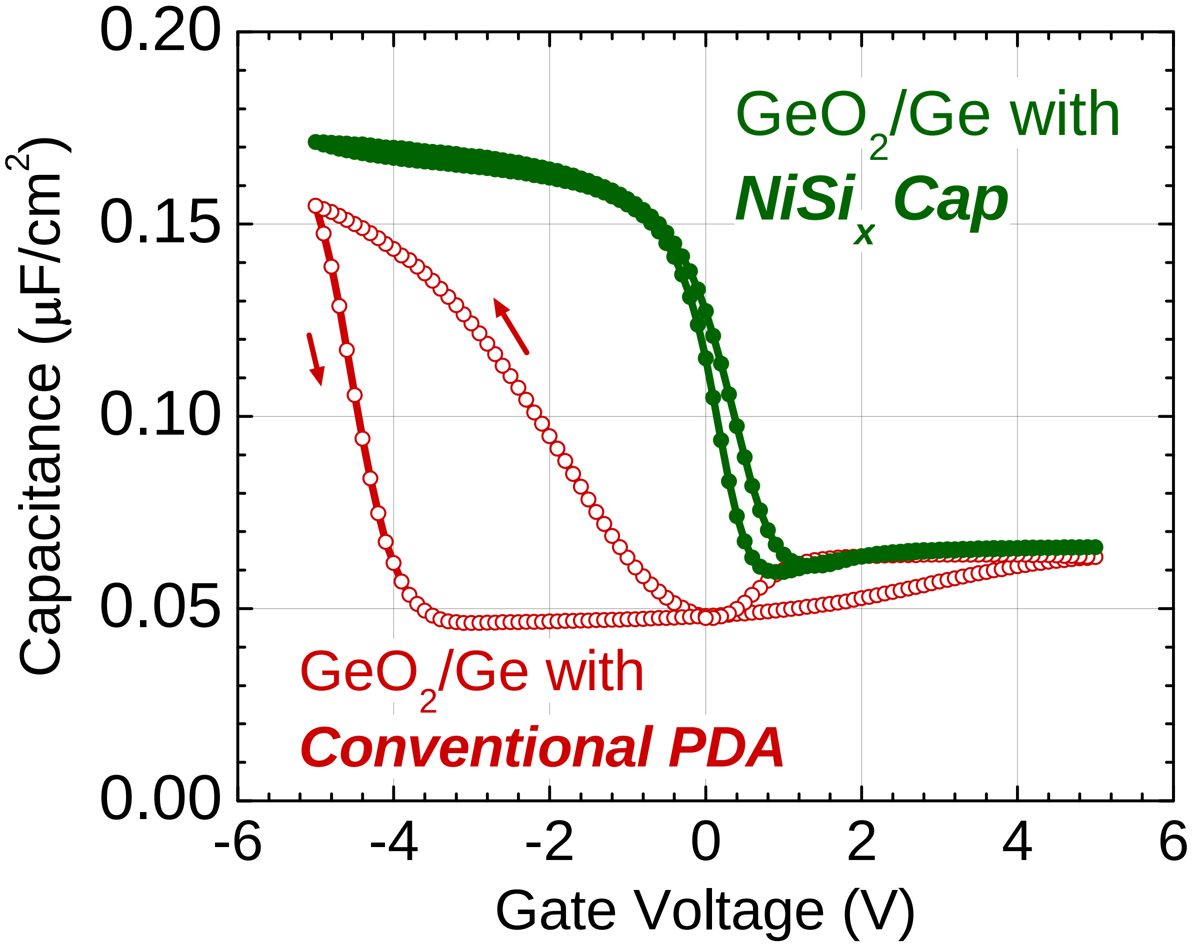
N_2 anneal at 600°C



Si capping layer can suppress GeO volatilization.

Dramatic Improvement of GeO_2/Ge MIS Characteristics with Capping Layer

（~25nm-thick GeO_2, after N_2 600°C anneal）



(1MHz)

S. Suzuki et al., SSDM 2007

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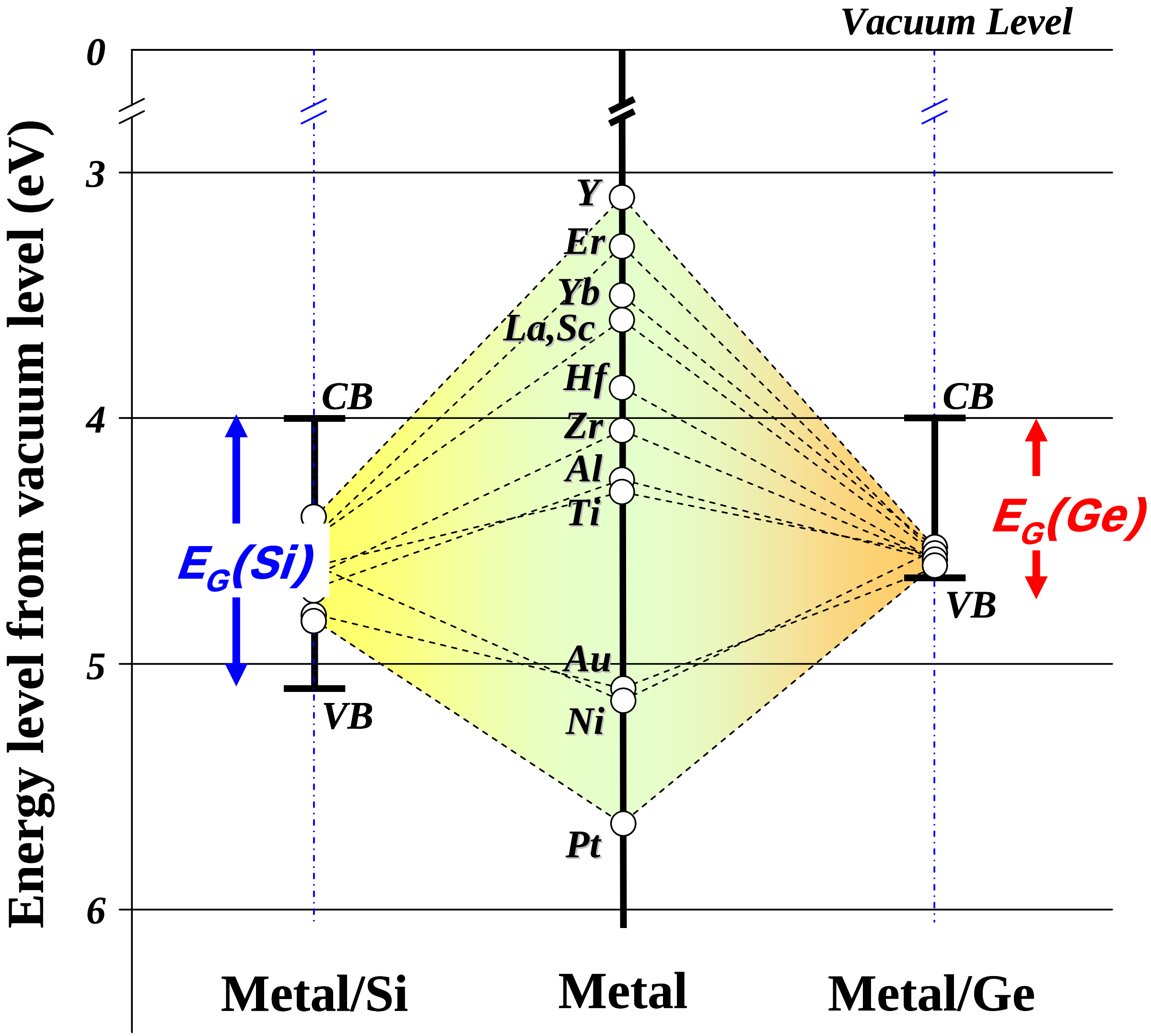
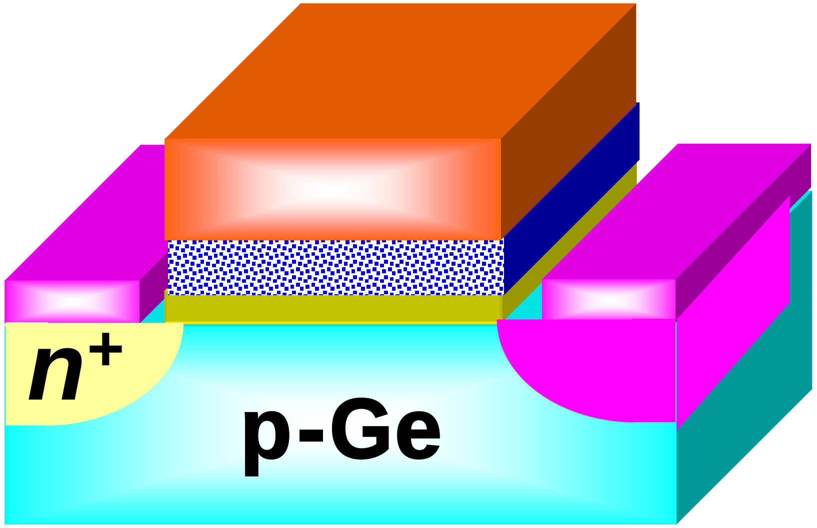
5. Conclusions

Strong Fermi-level Pinning at Metal/Ge





1) ***Metal source/drain***
2) ***Low ohmic contact resistance***

T. Nishimura et al., APL (2007)

Interface Modulation Effects

1. Forming gas annealing

Metal: Al

(annealing temp. 200~500°C)

2. Germanide reaction

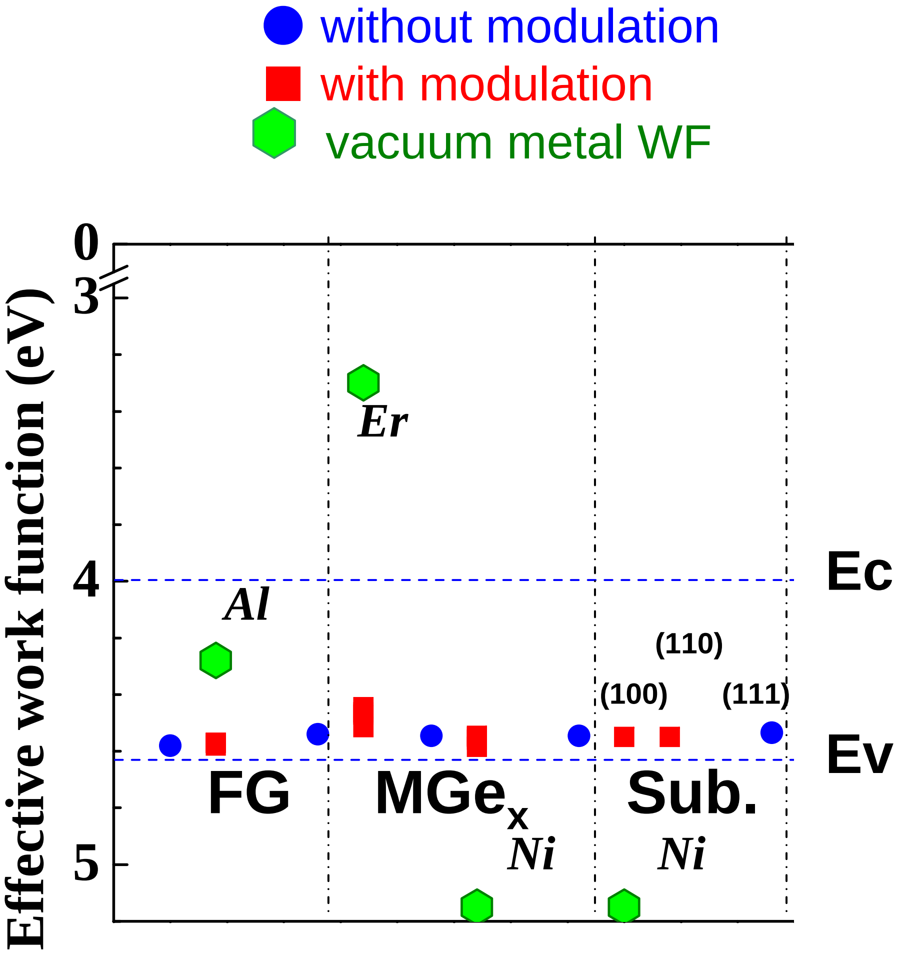
Metal: Er, Ni

(annealing temp. 200~500°C)

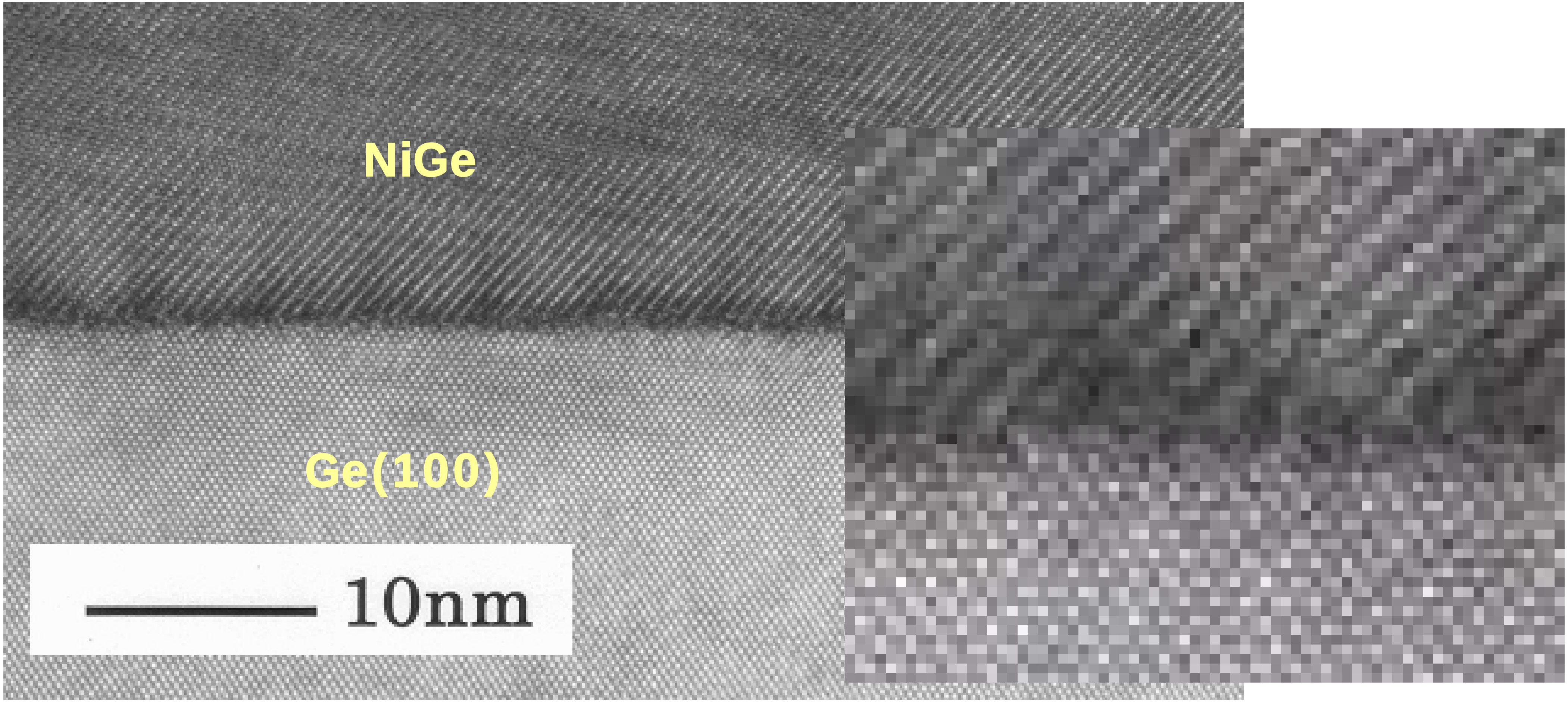
3. Substrate orientation

Metal: Ni

(Orientation:(100), (110), (111))

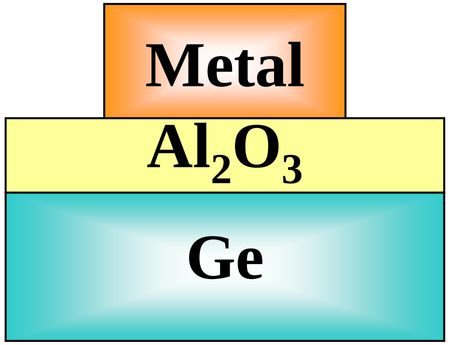


XTEM of NiGe/Ge(100) Interface

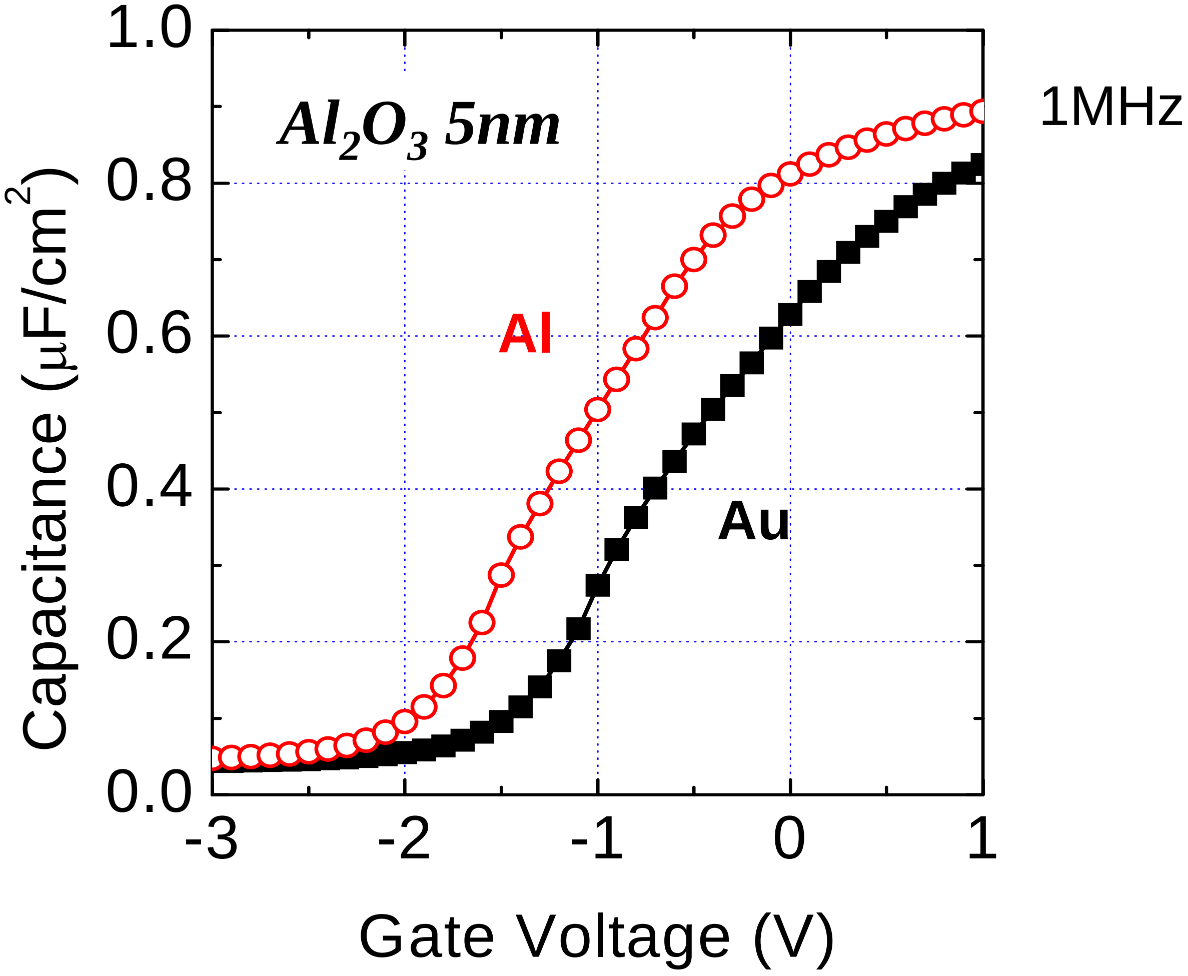


Still Strong Fermi level Pinning even after Reaction

Unpinned Ge MIS Capacitor



- ◆*Metal dependent V_{FB}*



No Fermi Level Pinning thanks to Insulator Insertion

Possible Origin of Fermi-level Pinning

Metal-induced Gap States (MIGS) Formation

- *Metal wave function penetration*
- *Ge intrinsic properties*

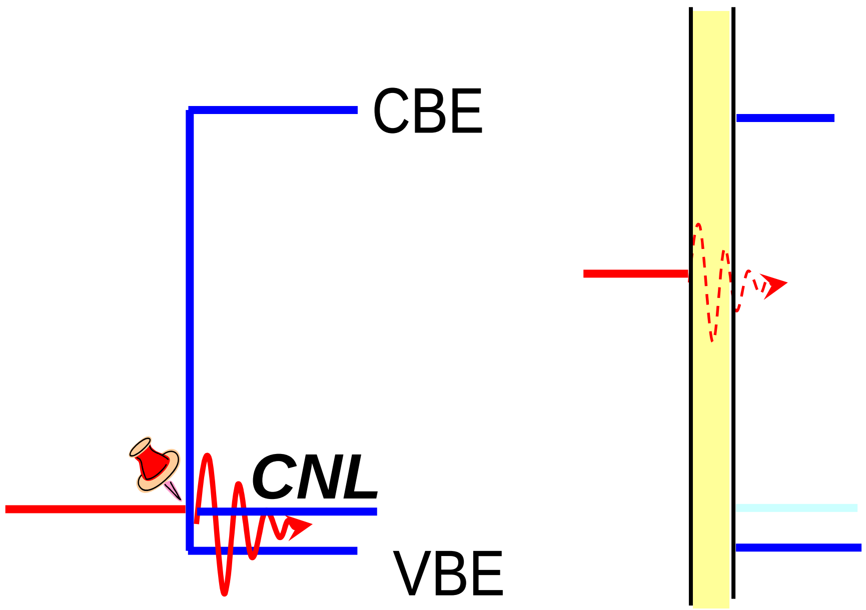
	CNL (This work)	Branch Point	
Ge	**4.58 eV**	**4.48***	**4.63****

	S_{exp}	S_{calc}
Ge	**0.02**	**0.04*****

J. Tersoff; PRL **32 (1984) 465.*

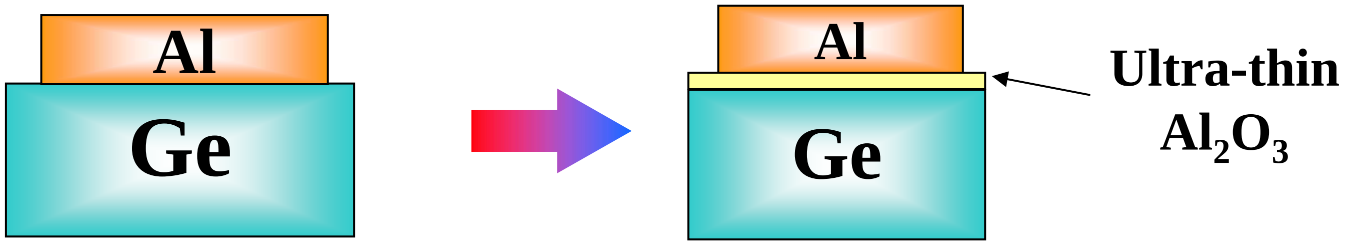
***M. Cardona and N. Christensen; PRB **35** (1987) 6182.*

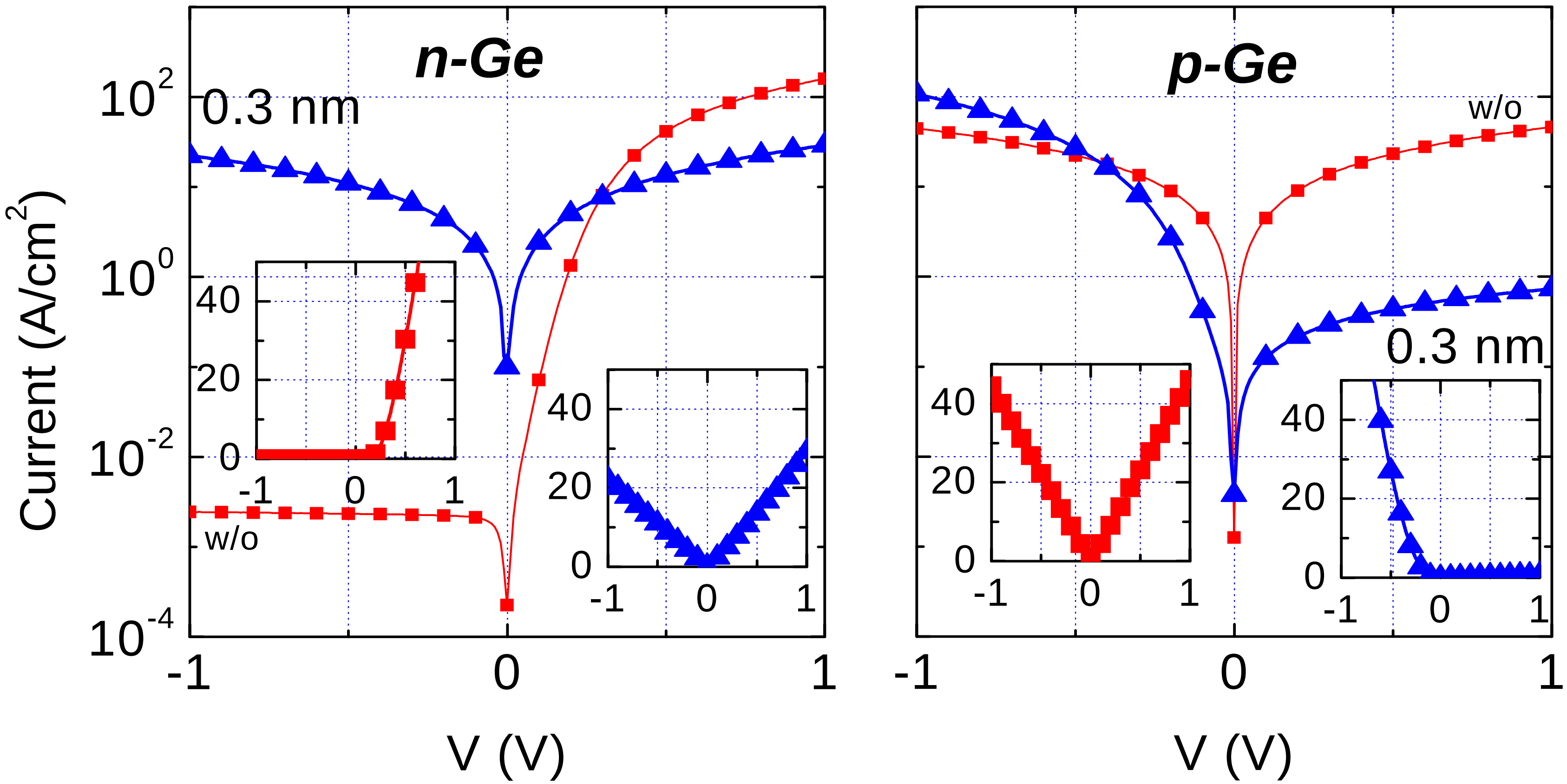
****W. Monch; JVST. B **17** (1999) 1867.*



T. Nishimura et al., APL (2007)

I-V Characteristics @Al/Ge





T. Nishimura et al., submitted.

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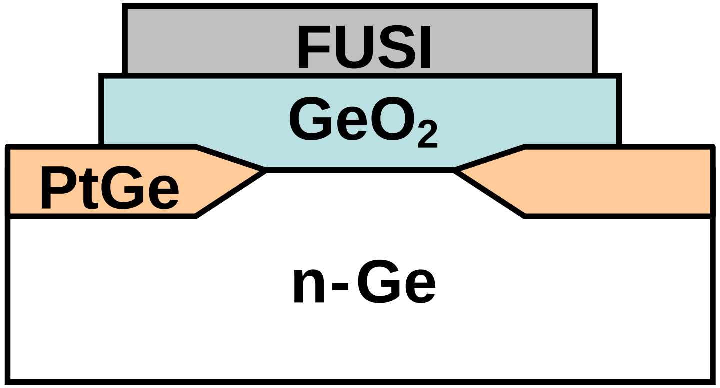
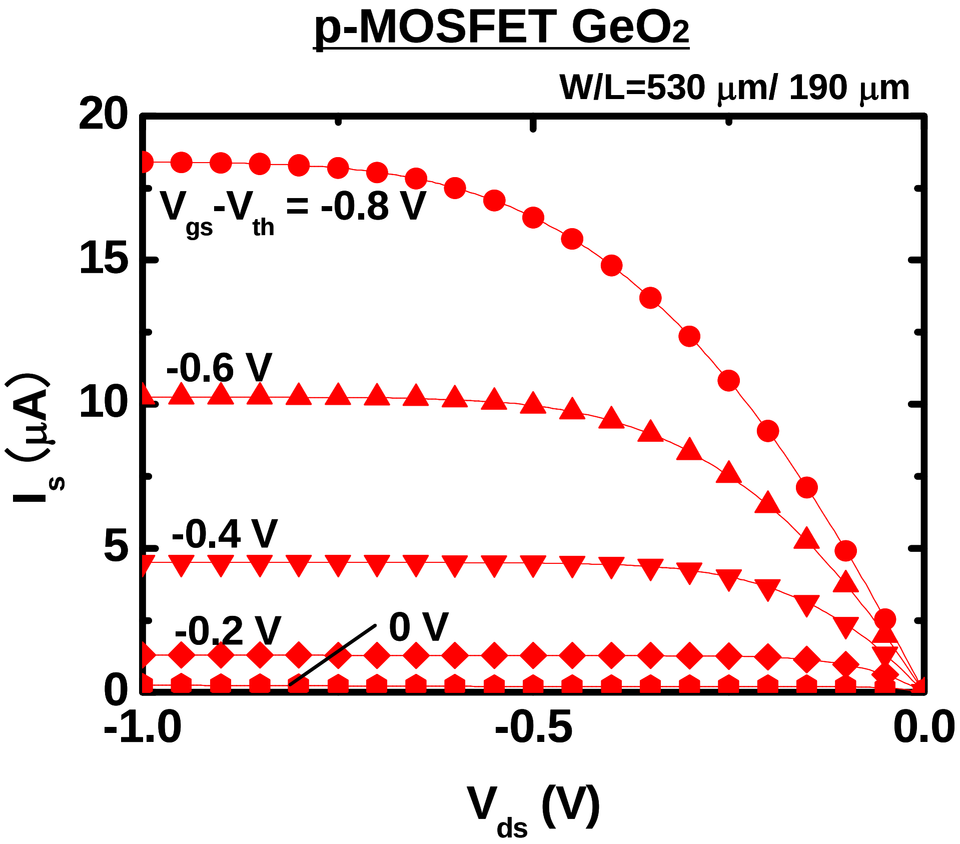
5. Conclusions

Metal source/drain p-ch Ge MOSFET

Metal source/drain p-ch Ge(100) MOSFET

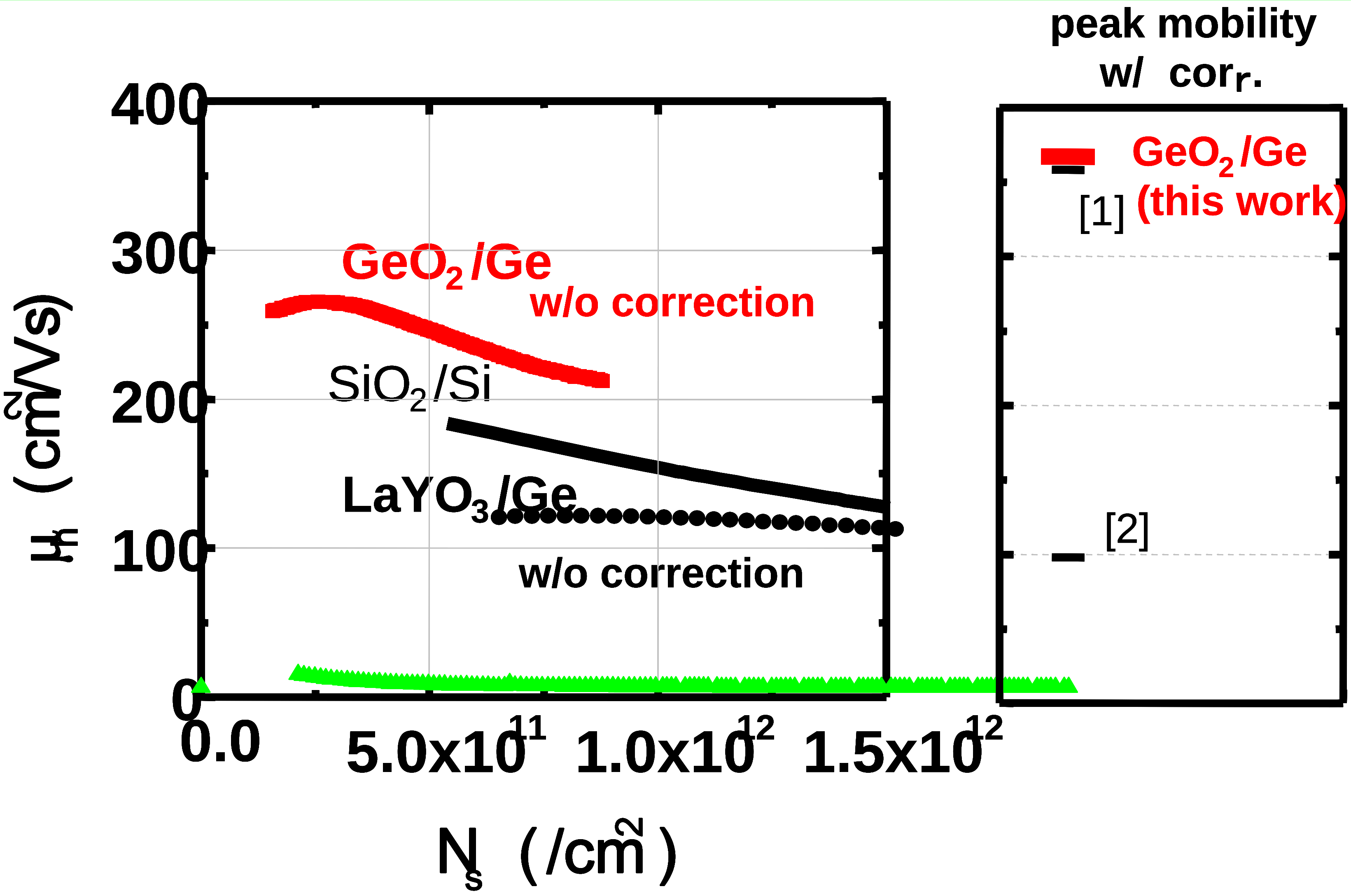




No Impurity Doping !

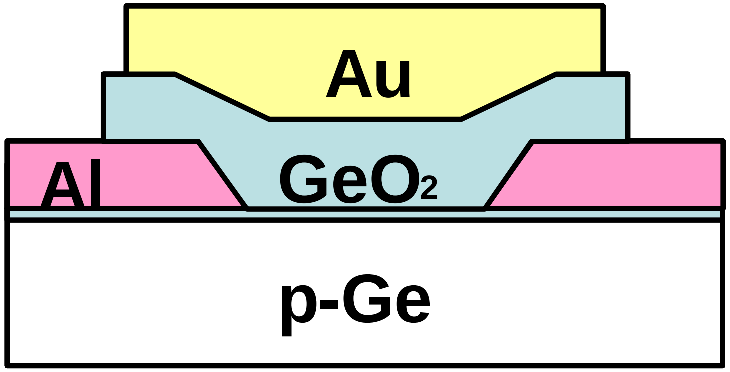
T. Takahashi et al., iedm2007

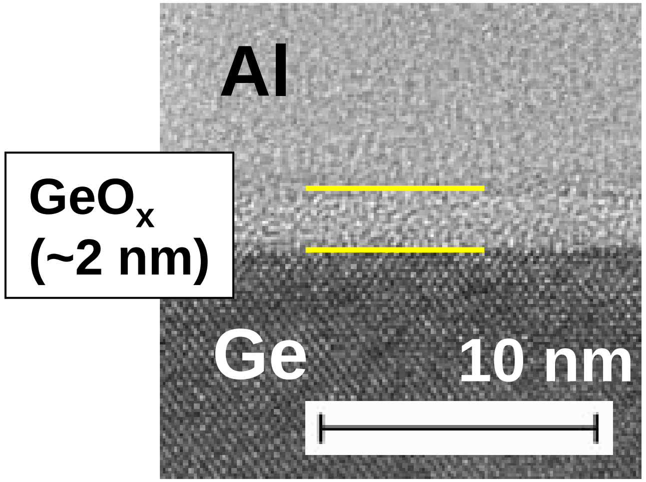
Inversion Hole mobility of Ge MOSFET



[1] P. Zimmerman et al., IEDM **2006**, 655, [2] W. Zhu et al., IEEE Trans. on Electron Devices **51**, 98 (2004)

Metal Source / Drain Ge n-FETs

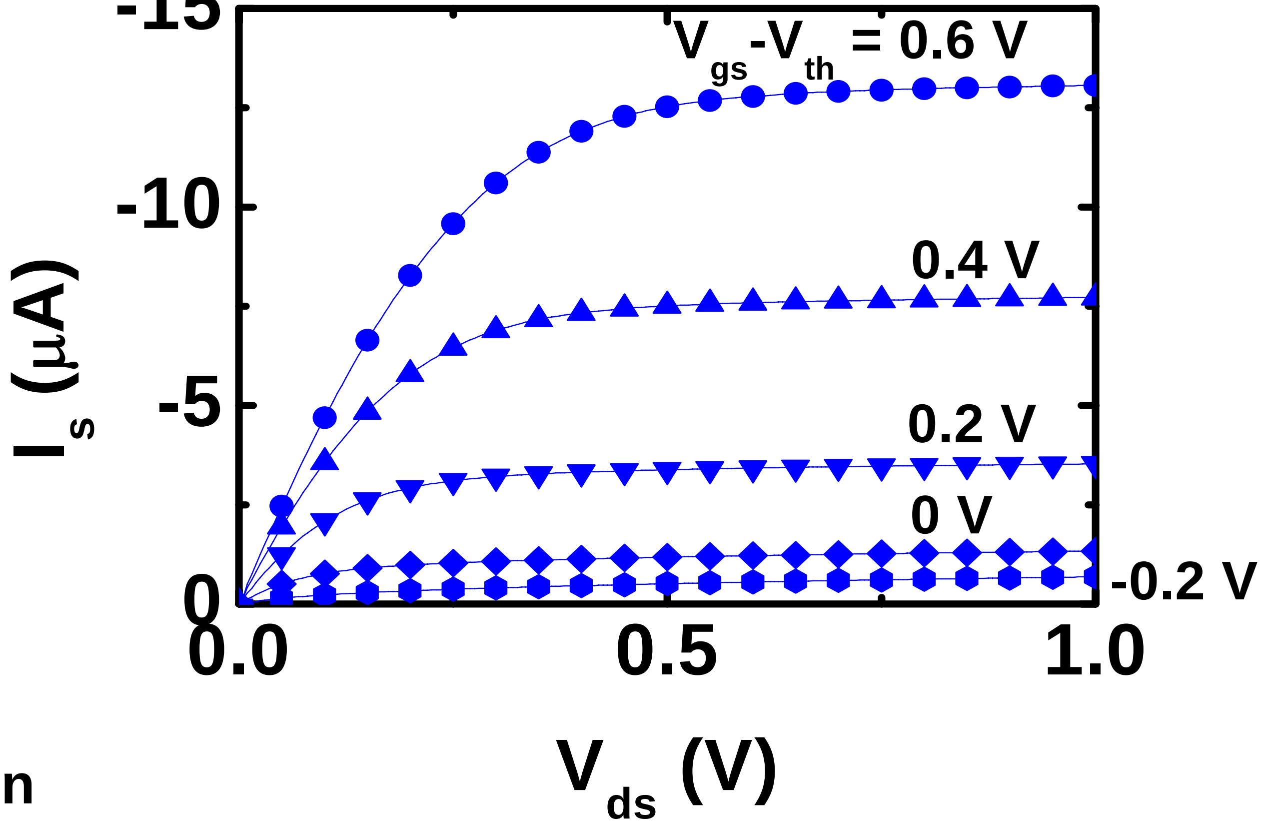




Schottky-Ohmic conversion with ultra-thin GeO_x

n-MOSFET GeO_2

W/L=530 μm/ 190 μm



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T. Takahashi et al., iedm2007

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Conclusions

- Origin of deterioration in GeO_2/Ge MIS is due to GeO desorption.
- GeO_2/Ge MIS can be dramatically improved by suppressing GeO volatilization with NiSi cap layer.

- Origin of FLP at Metal/Ge is attributable to metal-induced gap states (MIGS).
- Ultra-thin dielectric film insertion into metal/Ge can shift MIGS-related CNL.

- Metal source/drain Ge CMOS is coming soon.