Self-assembled SiGe islands: From fundamental perception to ultra large scale integration

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Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)

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(Received 27 December 1989)

We show that the islands formed in Stranski-Krastanow (SK) growth of Ge on Si(100) are initially *dislocation-free*. Island formation in true SK growth should be driven by strain relaxation in large, dislocated islands. Coherent SK growth is explained in terms of *elastic* deformation around the islands, which partially accommodates mismatch. The limiting critical thickness, h_c, of coherent SK islands is shown to be higher than that for 2D growth. We demonstrate growth of dislocation-free Ge islands on Si to a thickness of $\approx$ 500 Å, 50$\times$ higher than h_c for 2D Ge/Si epitaxy.

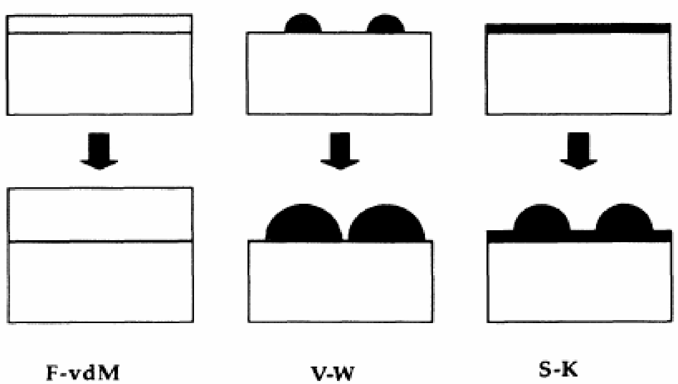


FIG. 1. Schematic diagram of the three possible growth modes: Frank–van der Merwe, Volmer-Weber, and Stranski-Krastinov. Where interface energy alone is sufficient to cause island formation, VW growth will occur; SK growth is uniquely confined to systems where the island strain energy is lowered by misfit dislocations underneath the islands.

500° C, 3 ML Ge

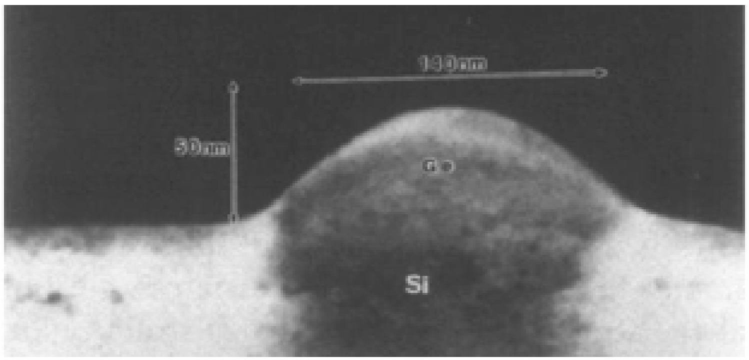


FIG. 4. Plan-view and cross-section TEM images of large coherent SK islands close to their maximum size prior to dislocation introduction. (a) Bright-field image near the {202} Bragg position showing characteristic "bend-contour" contrast due to dome-shaped deformation of the substrate around the island. (b) (400) dark-field image; note strong strain contrast around island.

Kinetic Pathway in Stranski-Krastanov Growth of Ge on Si(001)

Y.-W. Mo, D. E. Savage, B. S. Swartzentruber, and M. G. Lagally
University of Wisconsin–Madison, Madison, Wisconsin 53706
(Received 23 April 1990)

The transition from 2D to 3D growth of Ge on Si(001) has been investigated with scanning tunneling microscopy. A metastable 3D cluster phase with well-defined structure and shape is found. The clusters have a {105} facet structure. Results suggest that these clusters define the kinetic path for formation of "macroscopic" Ge islands.

475° C, > 3 ML Ge

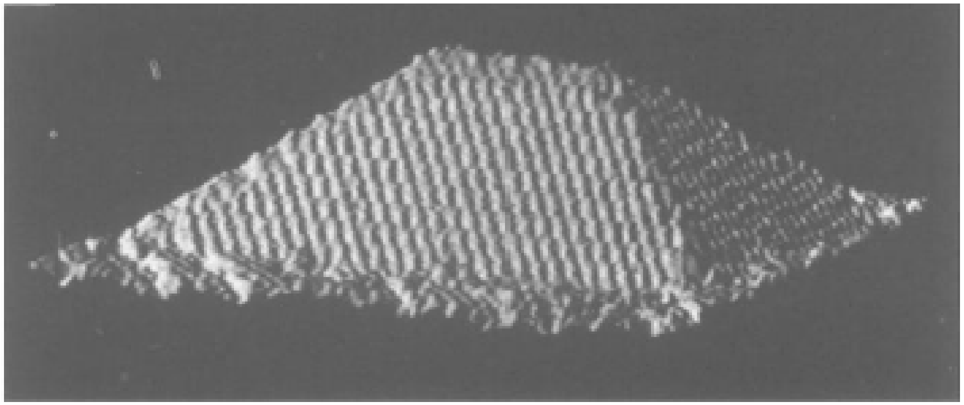
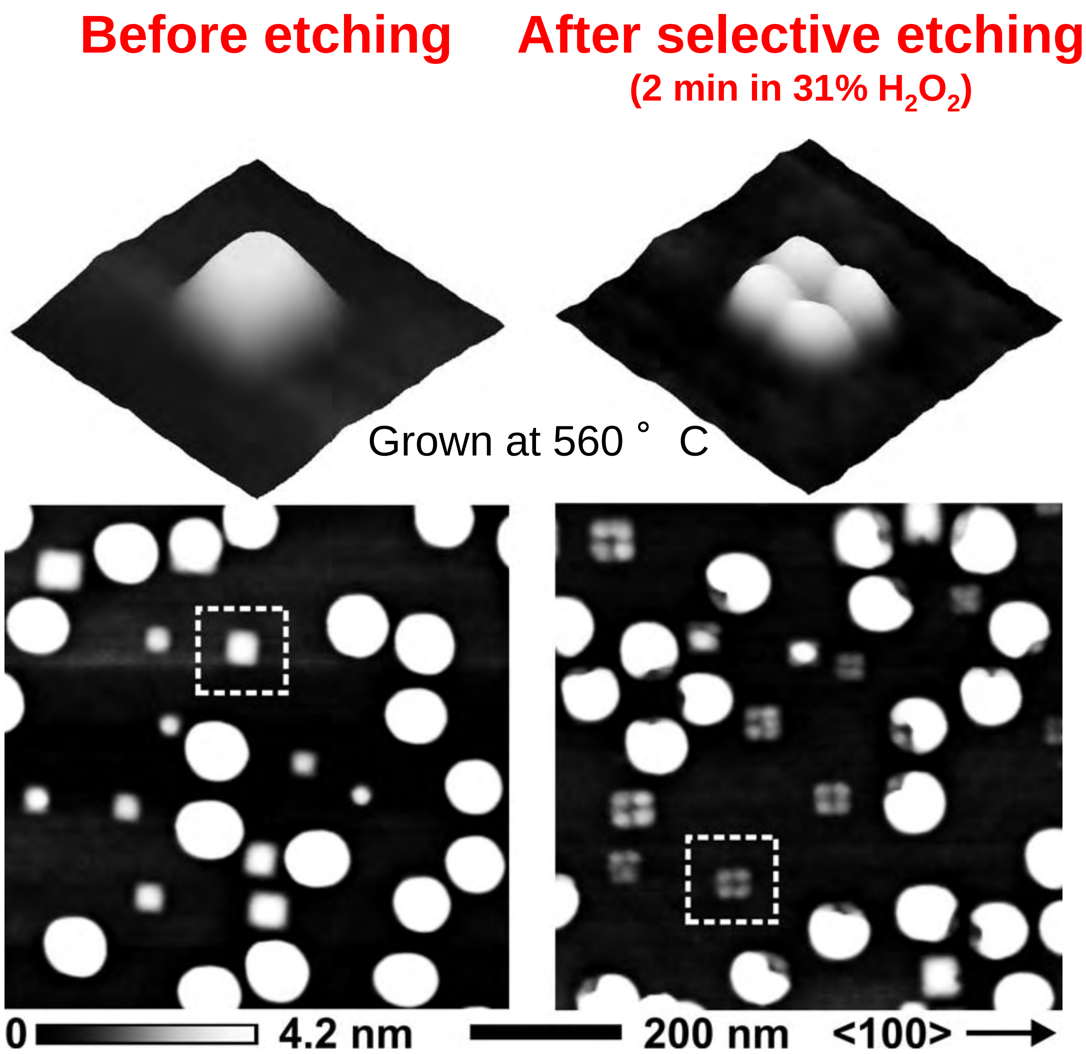
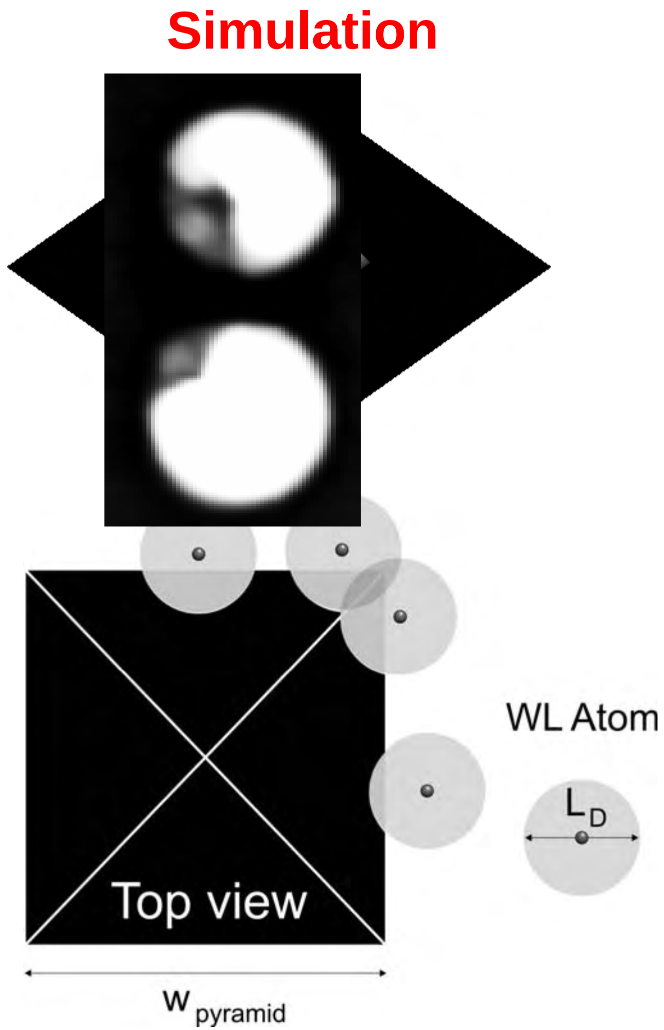


FIG. 2. STM images of single "hut" cluster. (a) Perspective plot. Scan area is 400 Å×400 Å. The height of the hut is 28 Å. (b) Curvature-mode grey-scale plot. The crystal structure on all four facets as well as the dimer rows in the 2D Ge layer around the cluster are visible. The 2D layer dimer rows are 45° to the axis of the cluster.

Probing the lateral composition profile of SiGe islands

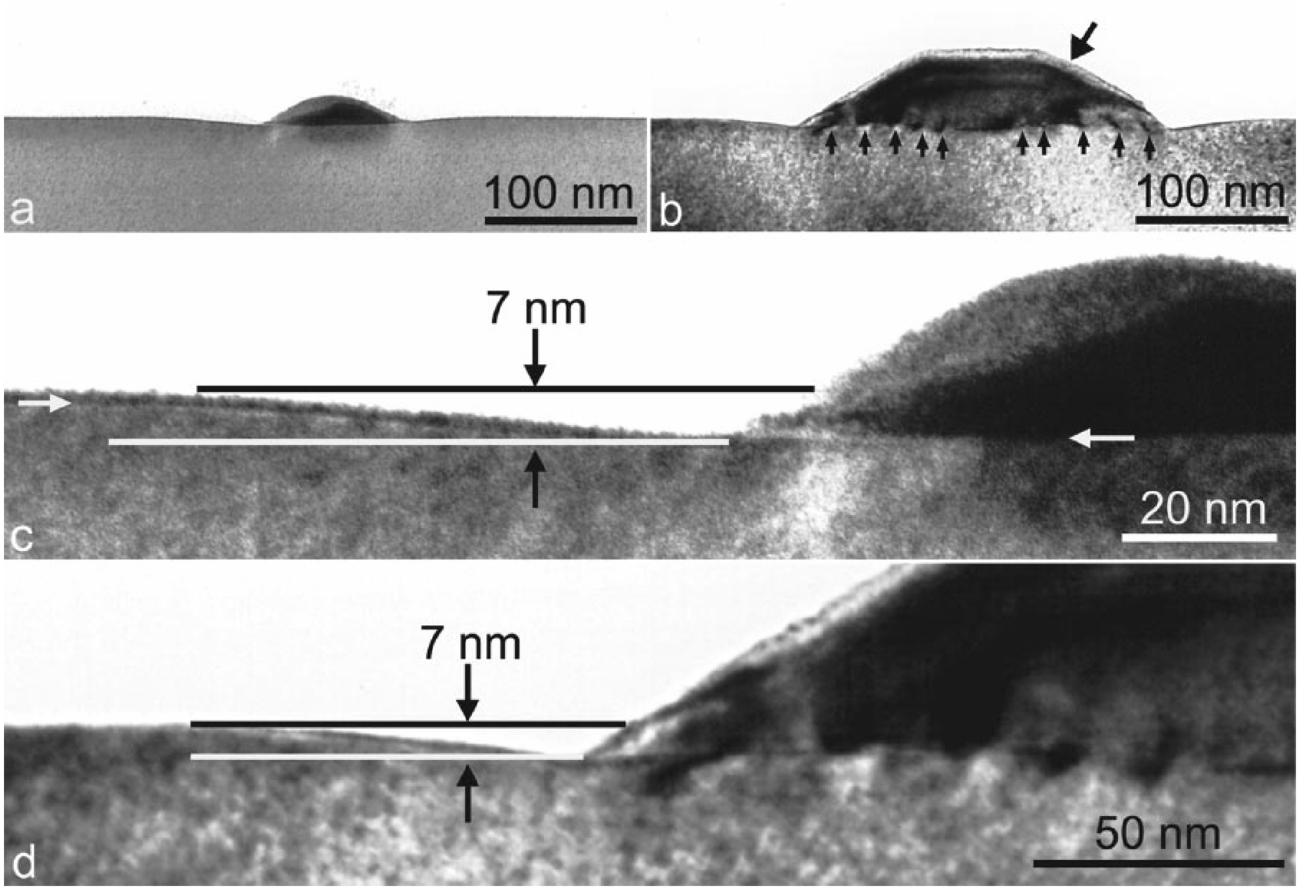




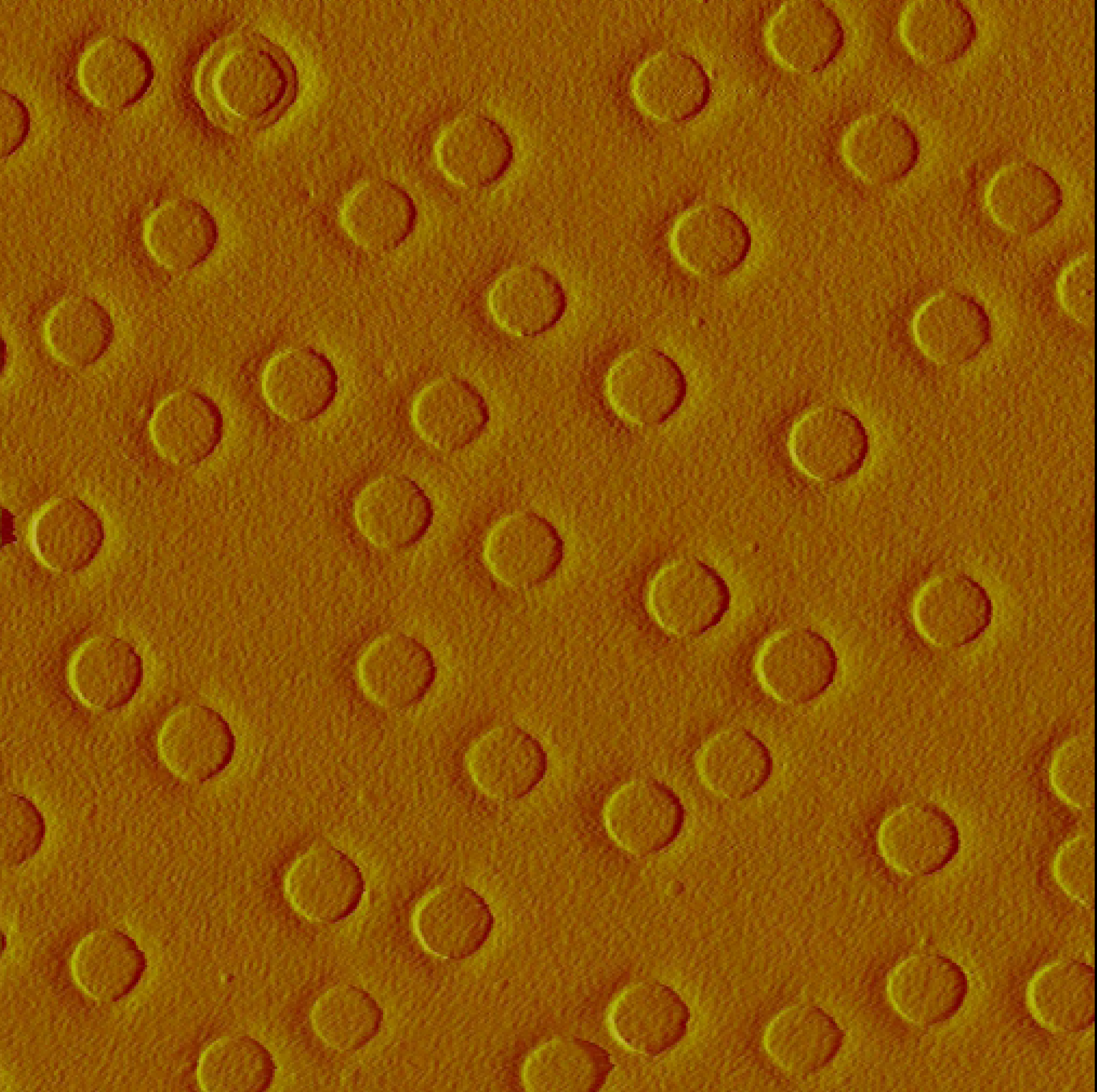
6 ML Ge at 560 °C, 500 s GI

U. Denker, M. Stoffel, and O. G. Schmidt, Phys. Rev. Lett. 90, 196102 (2003).

Trench formation around SiGe islands



X. Z. Liao et al., Phys. Rev. B 60, 15605 (1999)



2 x 2 μm^2

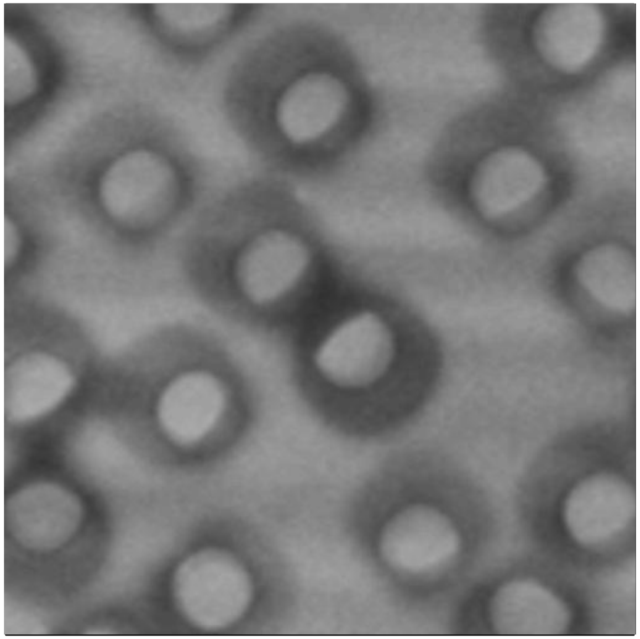
U. Denker et al.,
APL 78, 3723 (2001)

Trenches after post-growth annealing (in-situ)

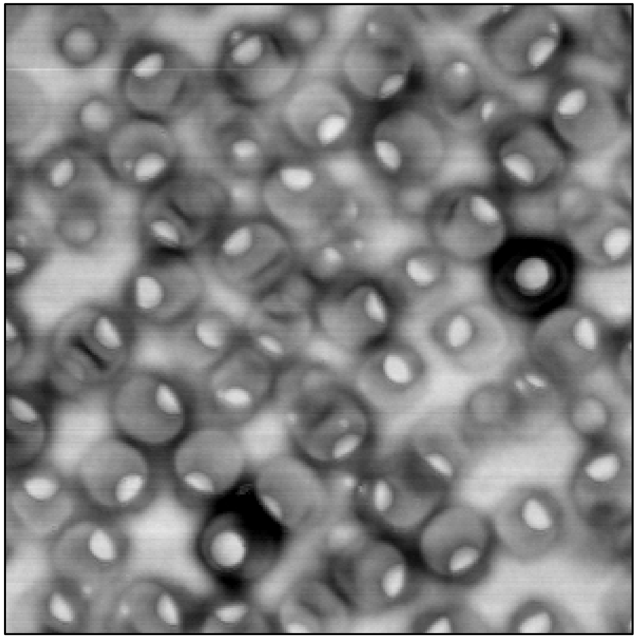
10 ML Ge at 740°C

After 2 min. etching in $HF/H_2O_2/CH_3COOH$ (BPA solution)

+ 1 min. anneal 740°C



+ 10 min. anneal 740°C



2.9 µm x 2.9 µm <110> →

- Before annealing: Si plateau at the center of the trench
- After annealing: only a part of the initial Si plateau remains and and a wide shallow trench appears

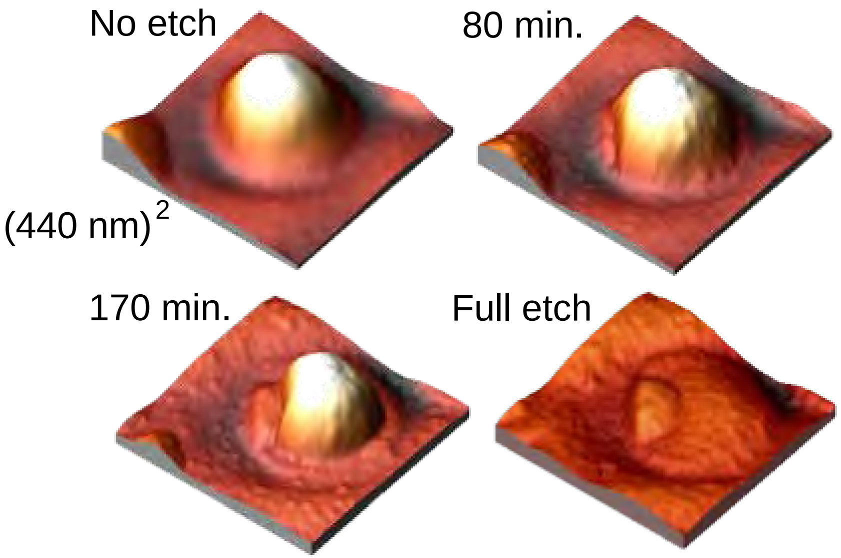
⇒ **Island motion**

Lateral SiGe island motion during in-situ annealing

U. Denker, A. Rastelli, M. Stoffel, J. Tersoff, G. Katsaros, G. Costantini, K. Kern, D. E. Jesson, and O. G. Schmidt, Phys. Rev. Lett. 94, 216103 (2005).

Evidence of asymmetric alloying

Wet chemical etching in a NH_4OH/H_2O_2 solution
(Etches Ge-rich SiGe alloys)

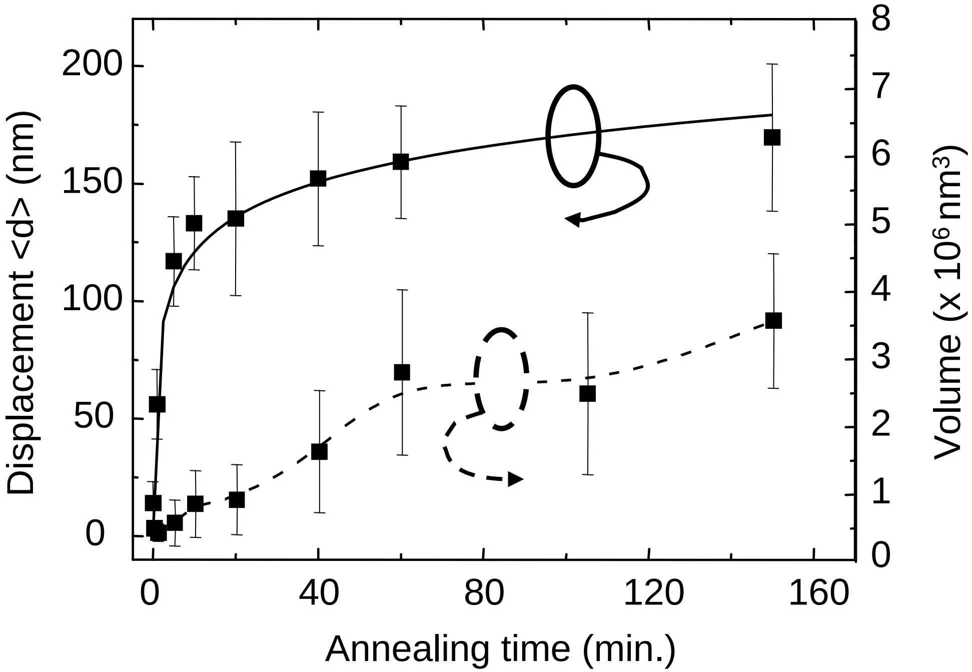


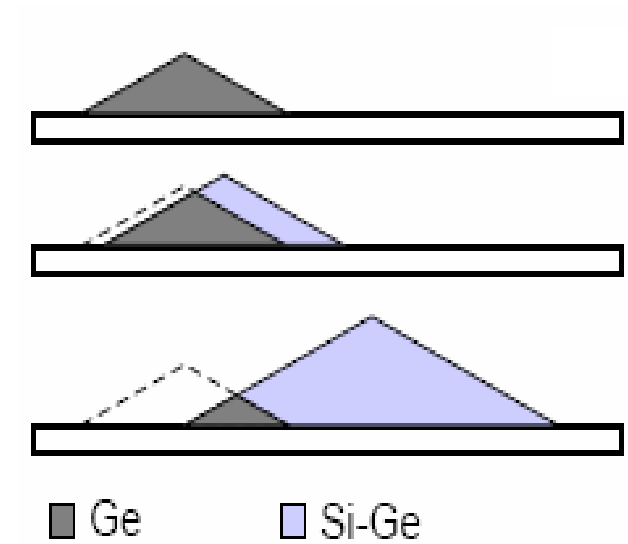
- Ge rich part at the left side of the island
- Si rich part at the right side of the island

Island motion: efficient Si-Ge intermixing by surface diffusion

Lateral SiGe island motion during in-situ annealing

Mean island displacement





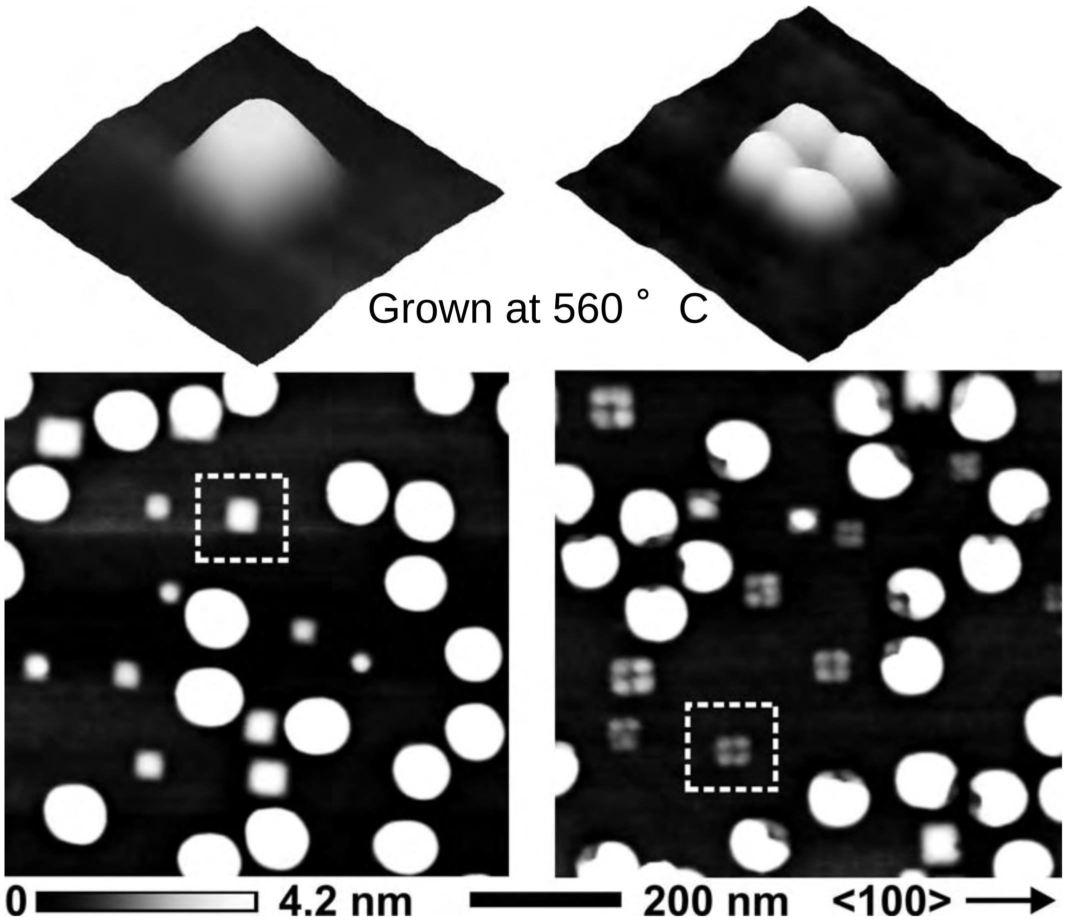
- Short annealing times: rapid island motion

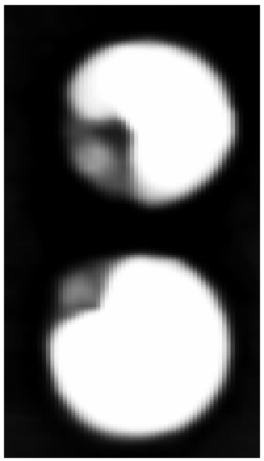
- Island motion slows down for annealing times > 20 min.

⇒ Once the island has intermixed, lateral motion ceases

Probing the lateral composition profile of SiGe islands

Before etching **After selective etching**
(2 min in 31% H_2O_2)





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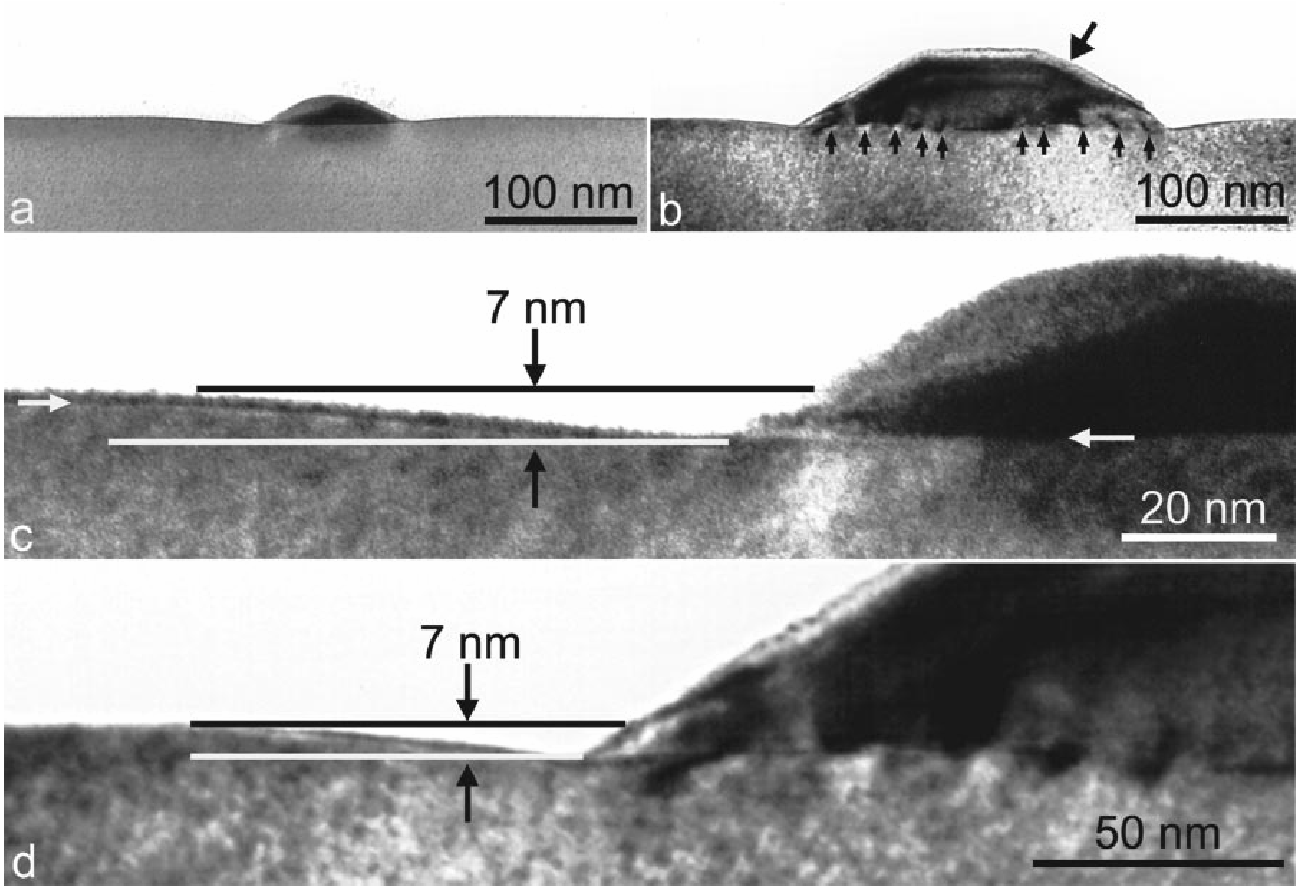
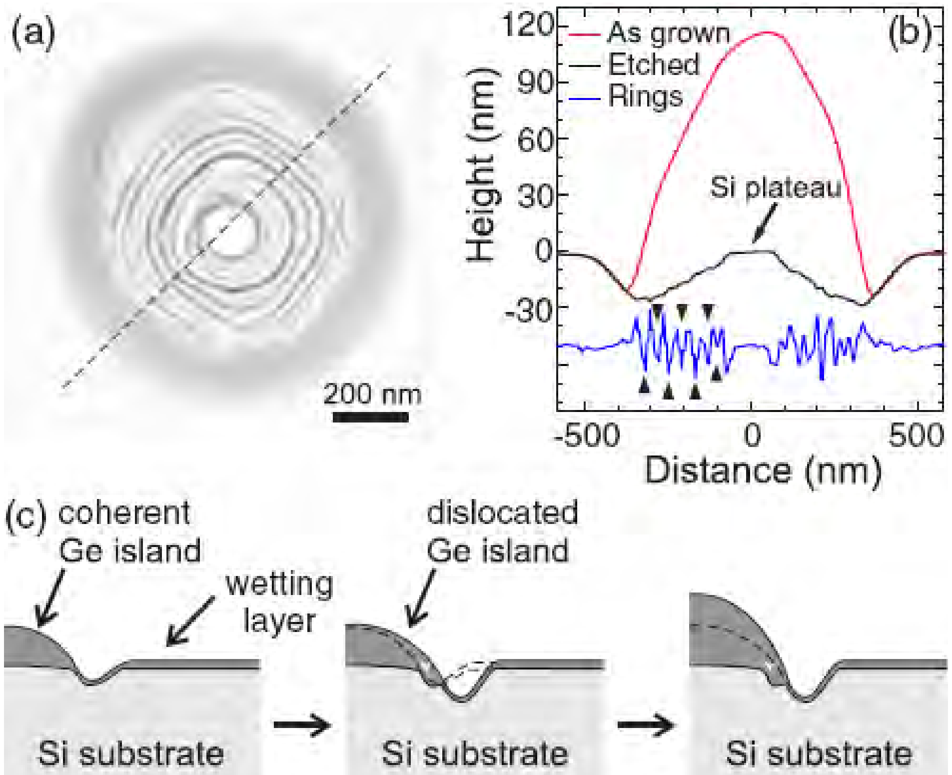
Trench formation around SiGe islands



X. Z. Liao et al., Phys. Rev. B 60, 15605 (1999)

Dendrochronology
(Study of tree-rings of dislocated superdomes)

SiGe islands



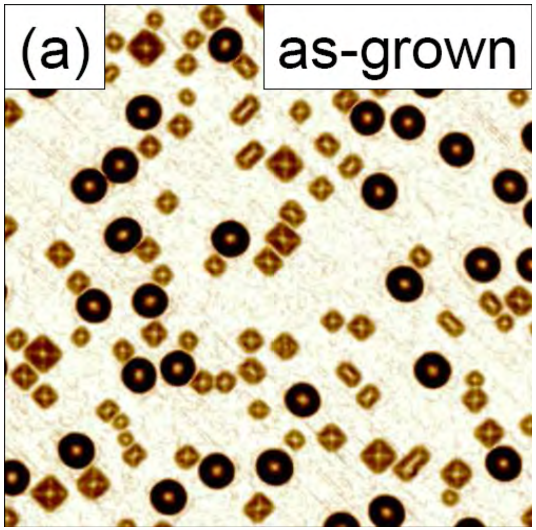
T. Merdzhanova, S. Kiravittaya, M. Stoffel, A. Rastelli, and O. G. Schmidt
Phys. Rev. Lett. 96, 226103 (2006)

Douglas-fir

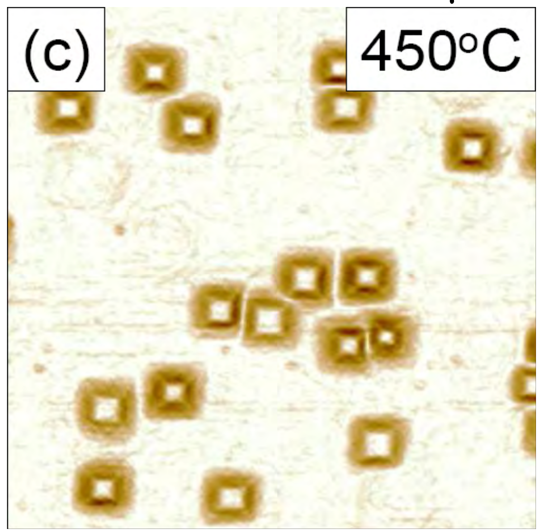
(photo H.D. Grissino-Mayer)

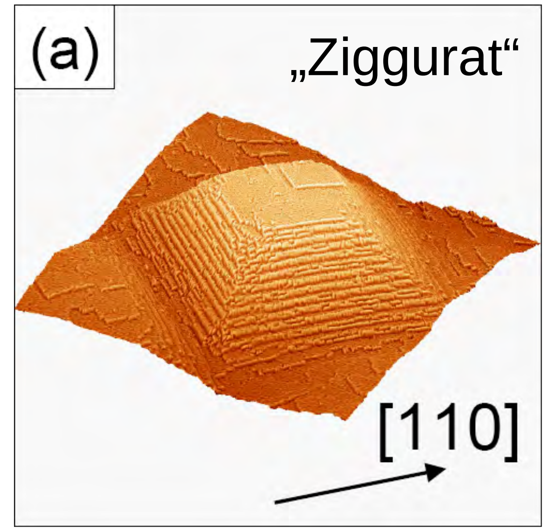
Revealing the details of capped SiGe islands

5.9 ML Ge, 580 °C

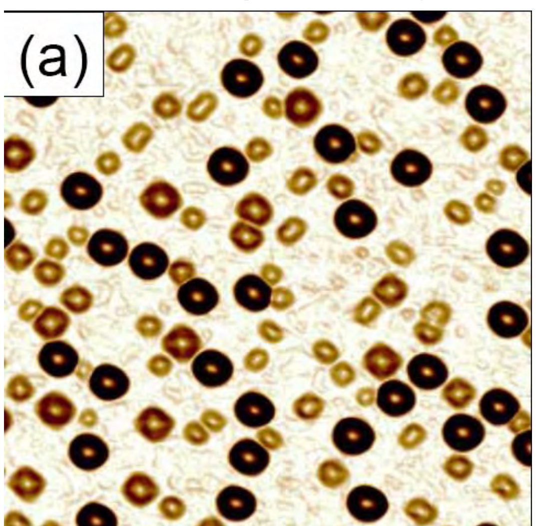


20 nm Si   2x2 μm^2

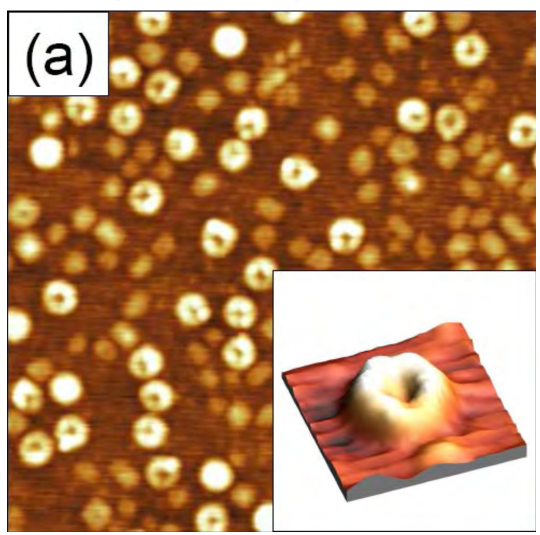




After Si cap etching



Composition profile

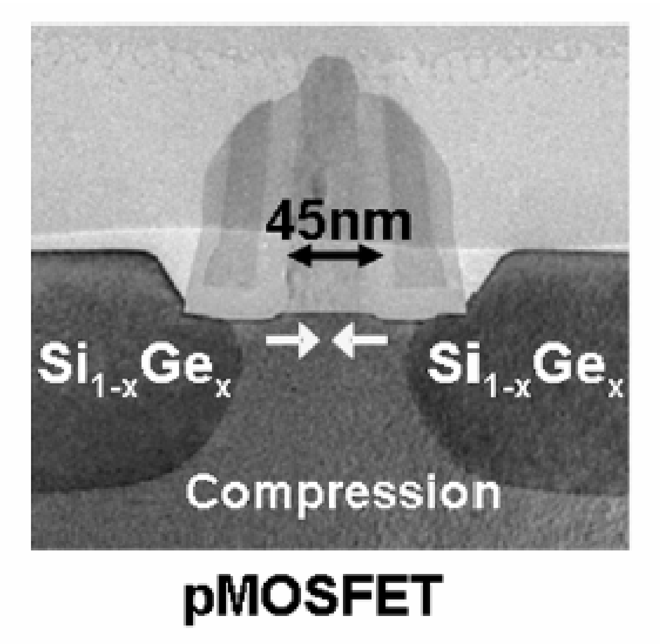


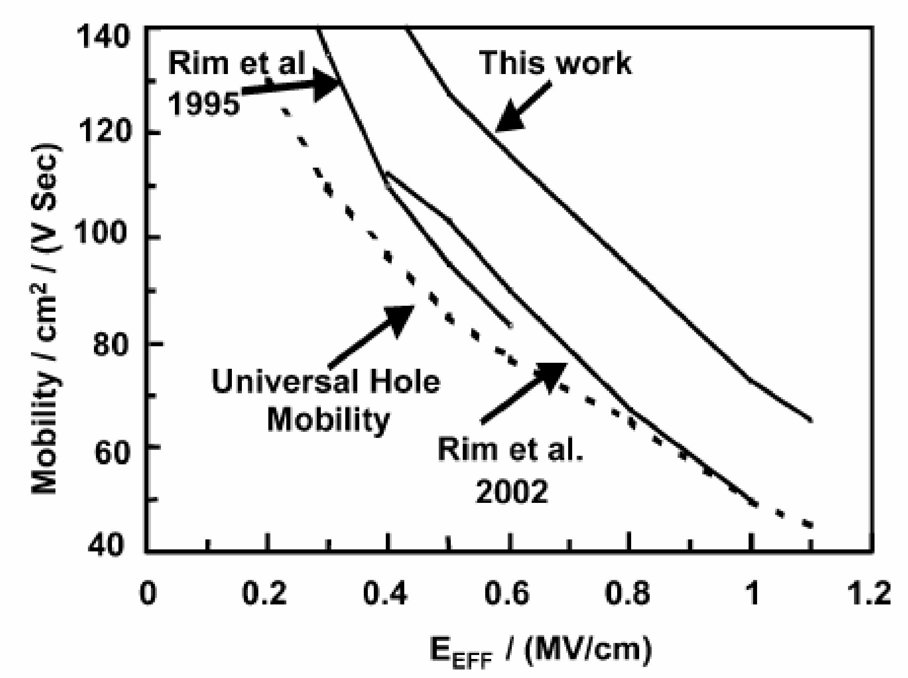
Although islands look completely different after capping, they remain practically unchanged below the Si !!!

G. Katsaros et al.,
APL 89, 253105 (2006)

A 90-nm Logic Technology Featuring Strained-Silicon

Scott E. Thompson, *Member, IEEE*, Mark Armstrong, Chis Auth, Mohsen Alavi, Mark Buehler, Robert Chau, Steve Cea, Tahir Ghani, Glenn Glass, Thomas Hoffman, Chia-Hong Jan, Chis Kenyon, Jason Klaus, Kelly Kuhn, Zhiyong Ma, Brian Mcintyre, Kaizad Mistry, *Member, IEEE*, Anand Murthy, Borna Obradovic, Ramune Nagisetty, Phi Nguyen, Sam Sivakumar, Reaz Shaheed, Lucian Shifren, Bruce Tufts, Sunit Tyagi, Mark Bohr, *Senior Member, IEEE*, and Youssef El-Mansy, *Fellow, IEEE*





➡ **However, low Ge concentration used (only 17 %)**

Difficult Challenges

Table PIDS1a Process Integration Difficult Challenges—Near-term Years

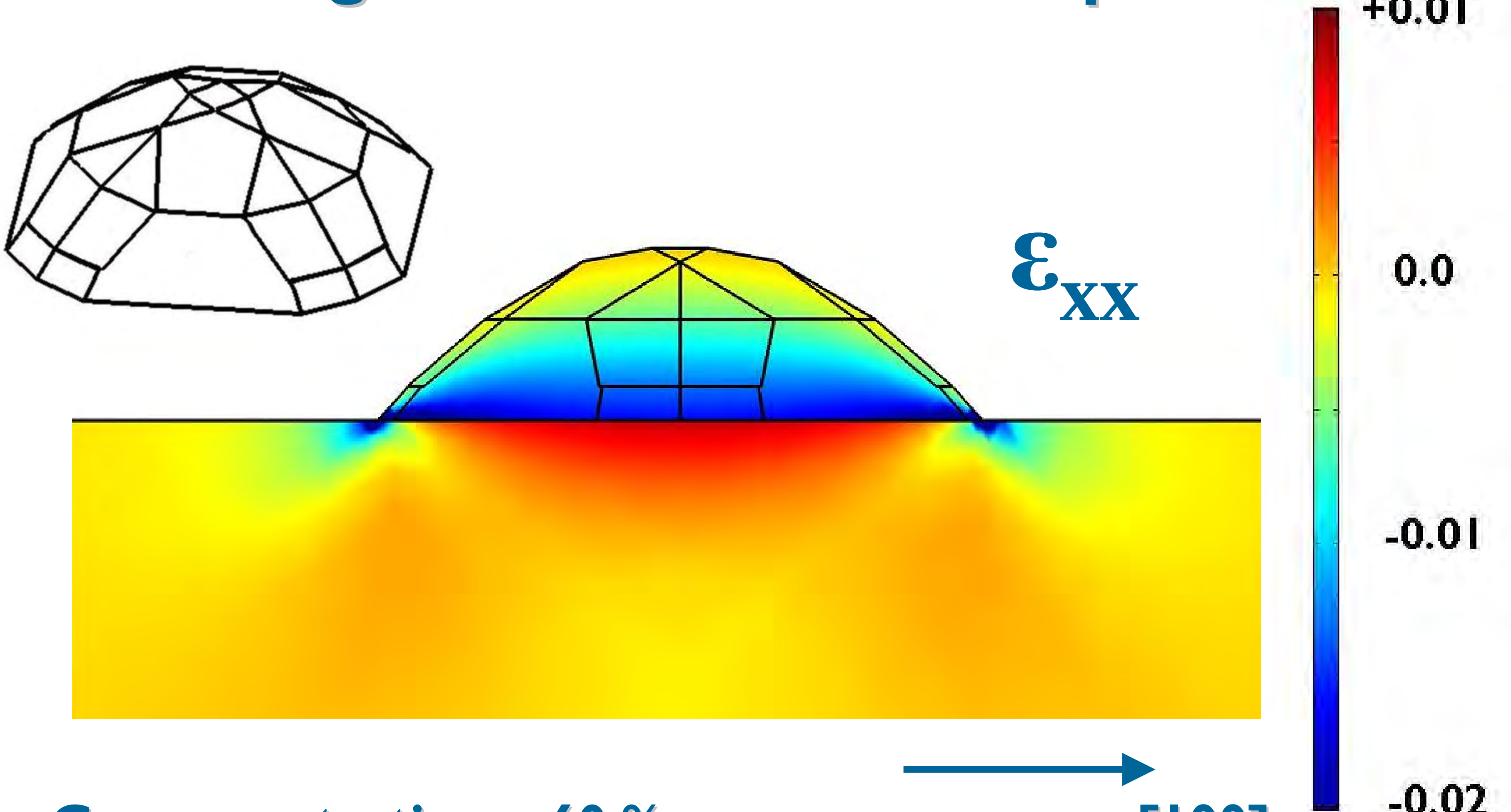
Difficult Challenges ≥ 22 nm	*Summary of Issues*
1. Scaling of MOSFETs to the 22 nm technology generation	Scaling planar bulk CMOS will face significant challenges due to the high channel doping required, band-to-band tunneling across the junction and gate-induced drain leakage (GIDL), random doping variations, and difficulty in adequately controlling short channel effects. Also, keeping parasitics, such as series source/drain resistance with very shallow extensions and fringing capacitance, within tolerable limits will be significant issues. Implementation into manufacturing of new structures such as ultra-thin body fully depleted silicon-on-insulator (SOI) and multiple-gate (e.g., FinFET) MOSFETs is expected at some point. This implementation will be challenging, with numerous new and difficult issues. A particularly challenging issue is the control of the thickness and its variability for these ultra-thin MOSFETs, as well as control of parasitic series source/drain resistance for very thin regions.
2. With scaling, difficulties in inducing adequate strain for enhanced mobility.	With scaling, it is critically important to maintain (or even increase) the current significantly enhanced CMOS channel mobility attained by applying strain to the channel. However, the strain due to current process-induced strain techniques tends to decrease with scaling.

„…as the spacing between transistors is reduced with scaling, techniques such as embedded SiGe or Si:C in the source/drain …becomes less effective at inducing stress in the channel.“

(ITRS 2007 edition)

ITRS: **I**nternational **T**echnology **R**oadmap for **S**emiconductors

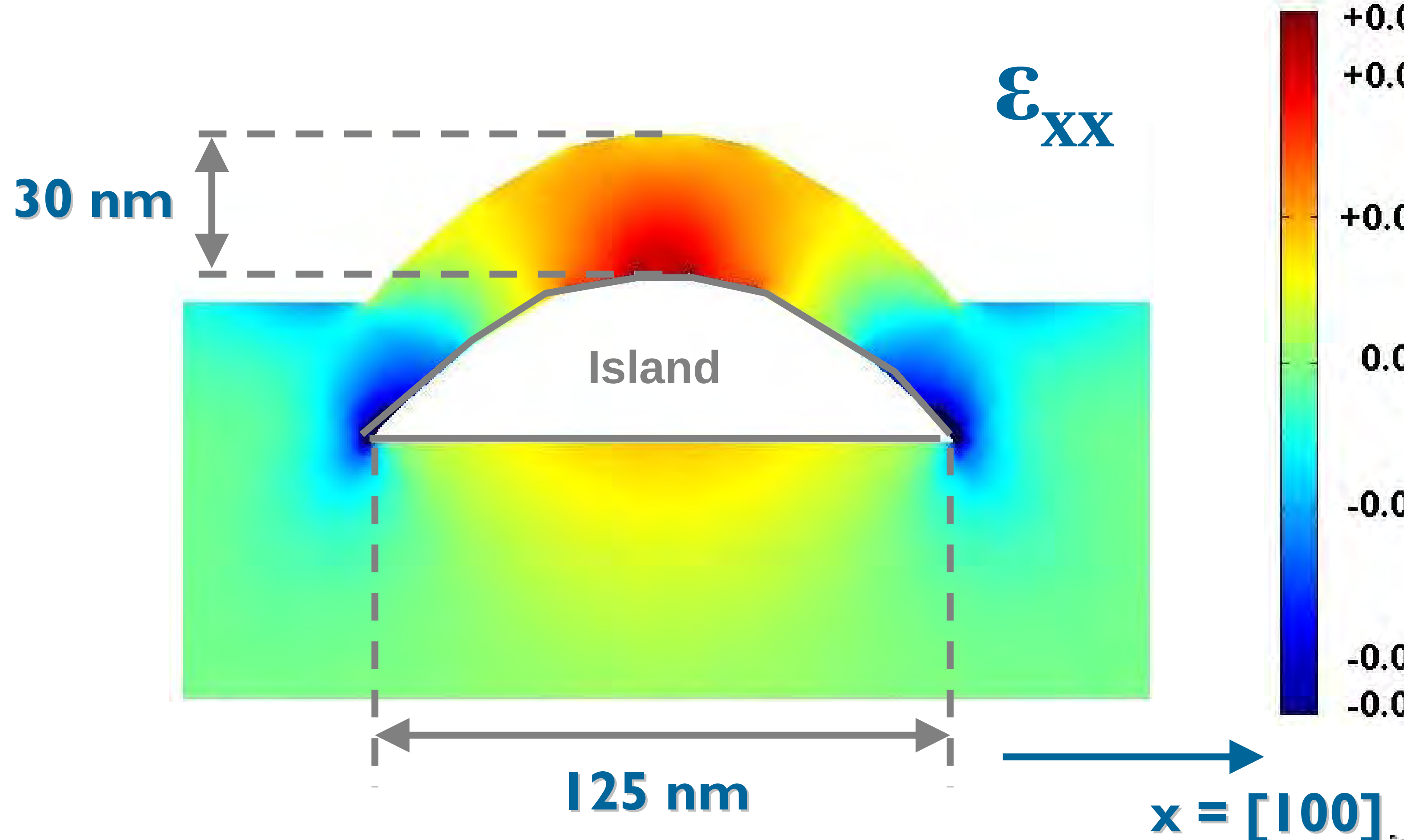
Modeling the realistic barn-shaped island



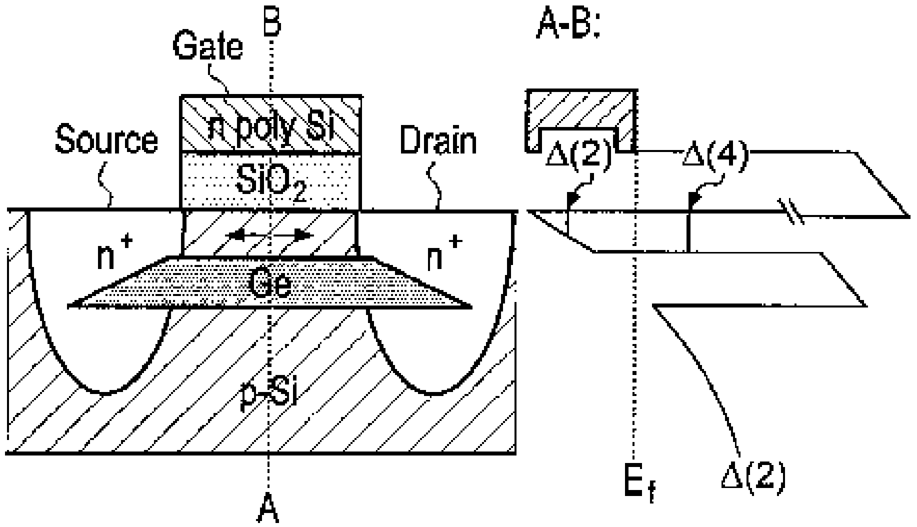
Ge concentration = 60 %

x = [100]

Strain induced in capping layer



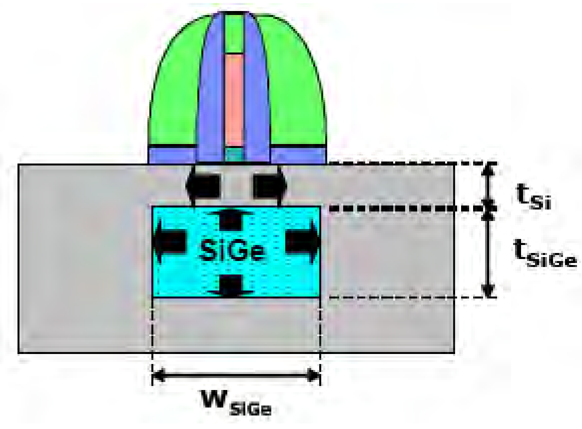
Field Effect Transistor based on embedded SiGe island structures (DotFET)



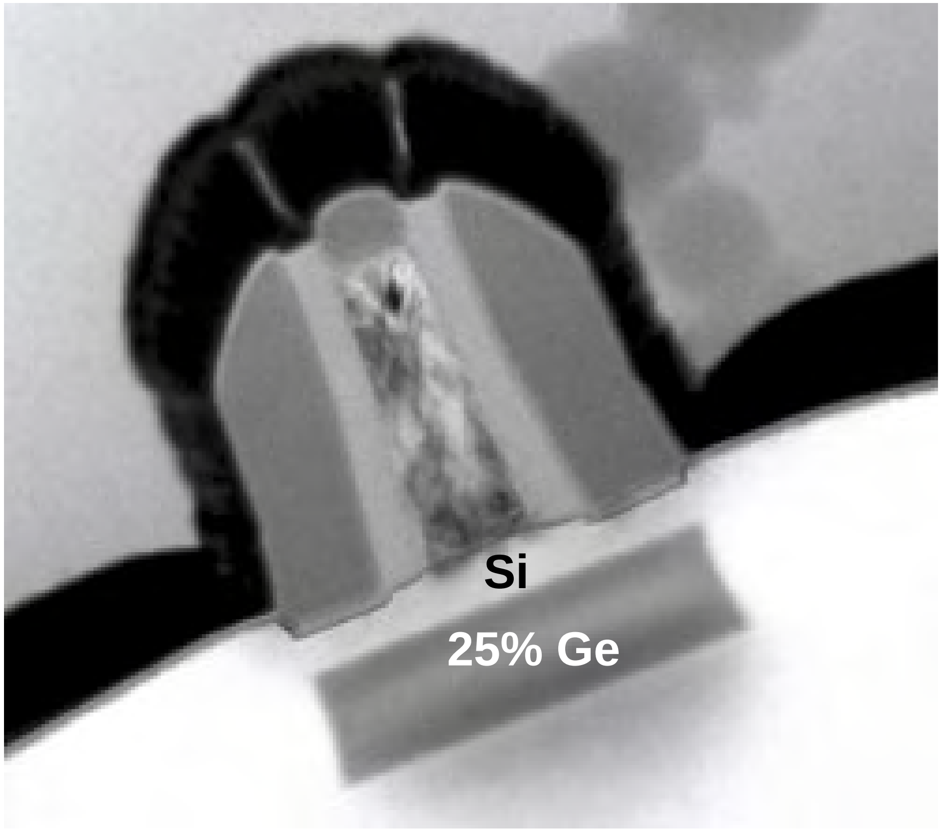
O. G. Schmidt and K. Eberl, US 6,498,359 (2000)
IEEE Trans. Electron. Devices 48, 1175 (2001)

MOSFET: The key device for ULSI technology.

„Reverse embedded SiGe“



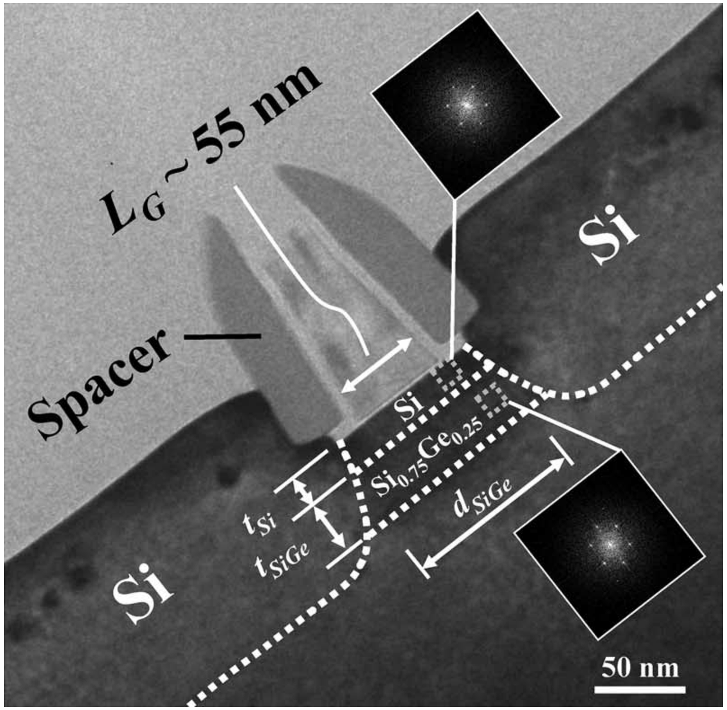
R. A. Donaton et al. (IBM),
IEDM Tech. Dig.,2006, pp. 465.



A buried SiGe island is very effective at inducing uniaxial tensile strain in the nFET channel for a 15% improvement in drive current and 40% mobility enhancement. The TEM shows the device following silicon regrowth in the source/drain. (Source: IBM)

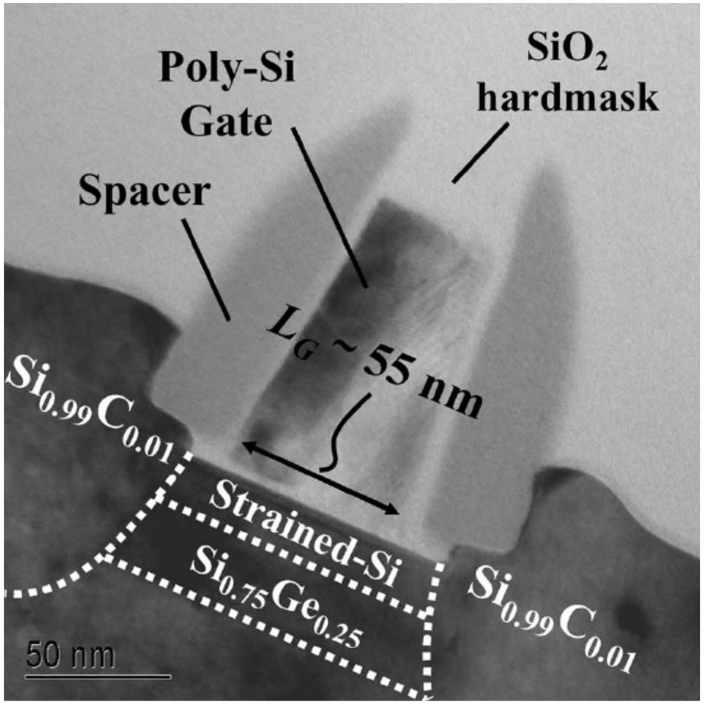
„SiGe strain transfer structure“

Single stressor



18% improvement in drive current
40% improvement of mobility

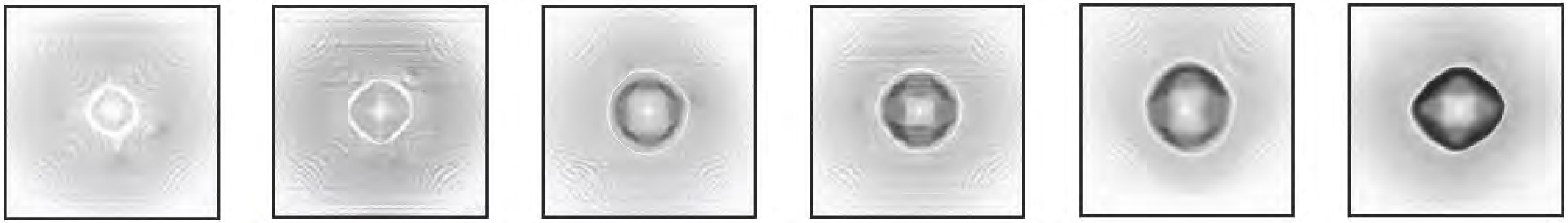
Dual stressor (Added Carbon)

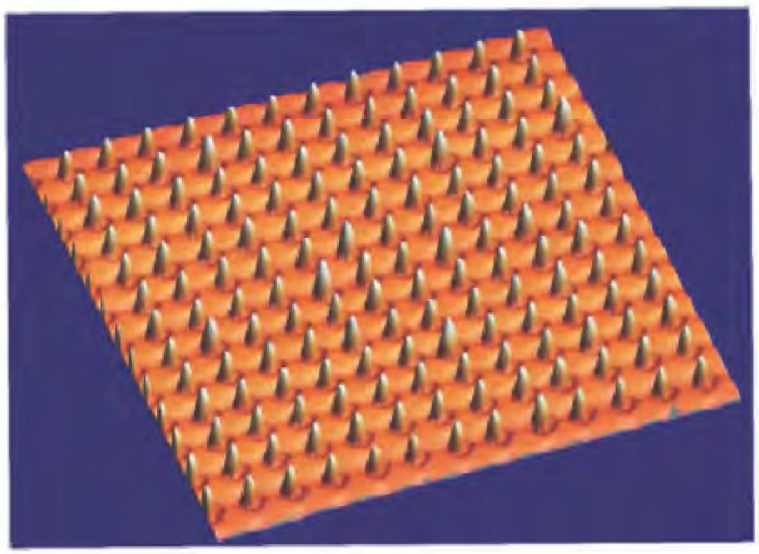


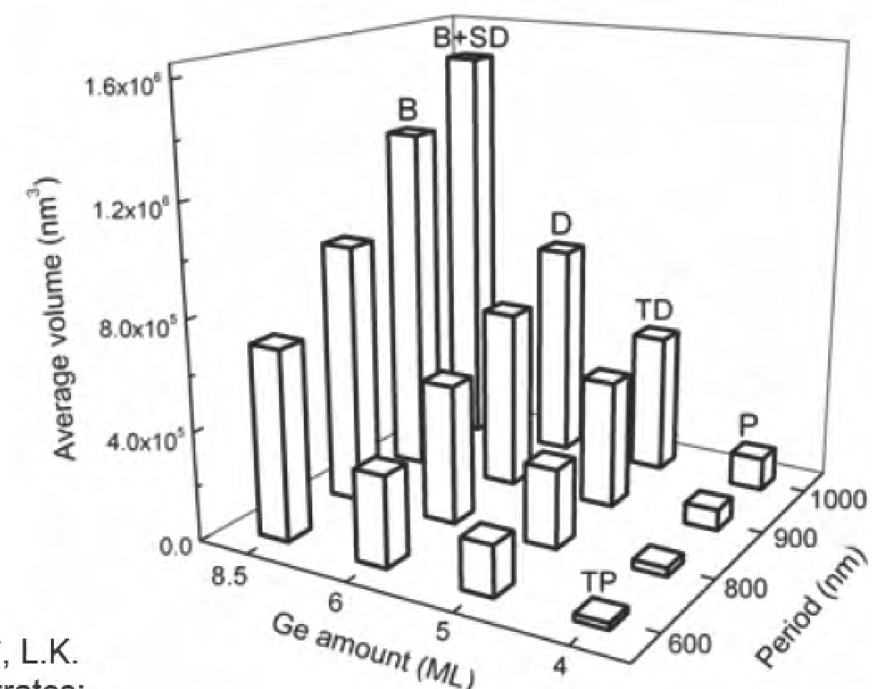
40% improvement in drive current
78% improvement of mobility

K.W. Ang et al., IEEE Electron Device Lett. 28, 609 (2007)
K.W. Ang et al., IEEE Trans. Electr. Devices 55, 850 (2008)

Perfect ordering of SiGe islands





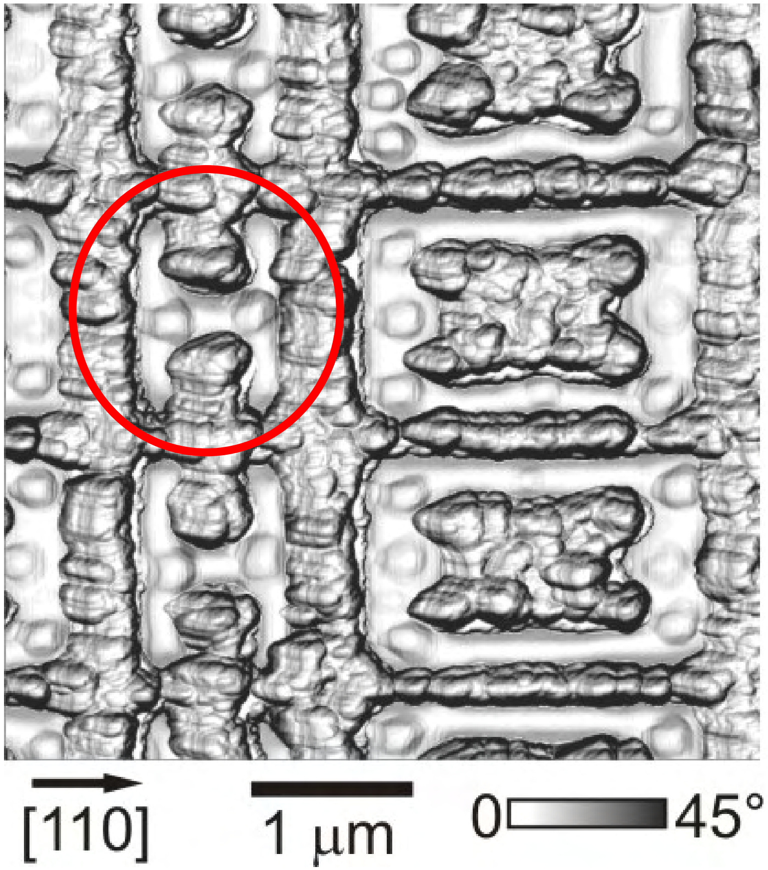


J. J. Zhang, M. Stoffel, A. Rastelli, O. G. Schmidt, V. Jovanovi*, L.K. Nanver, and G. Bauer, SiGe growth on patterned Si(001) substrates: Surface evolution and evidence of modified island coarsening, **Appl. Phys. Lett. 91, 173115 (2007)**

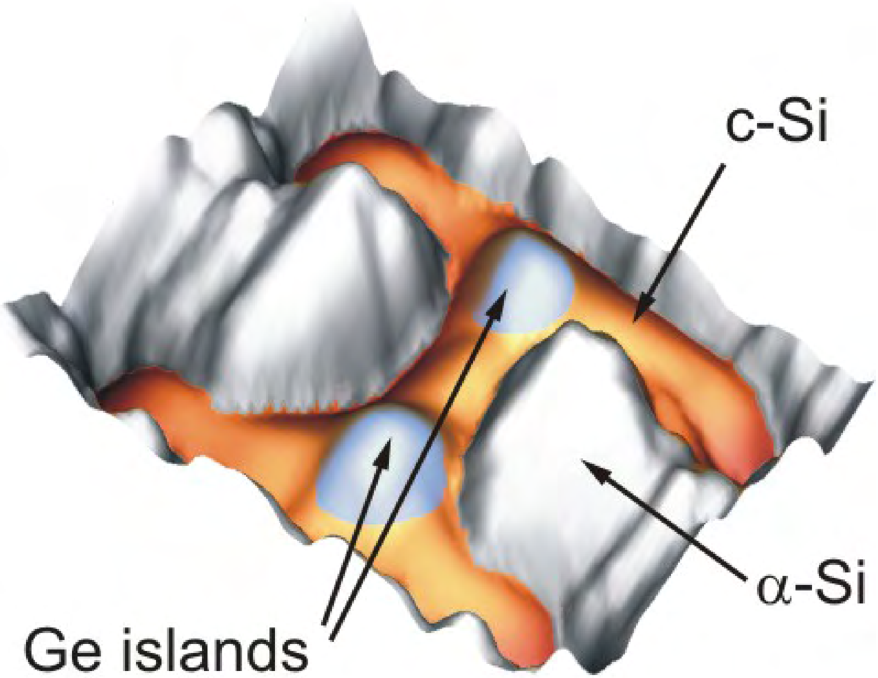
Funded by: EU project D-DotFET

Ge dot positioning on CMOS compatible wafers

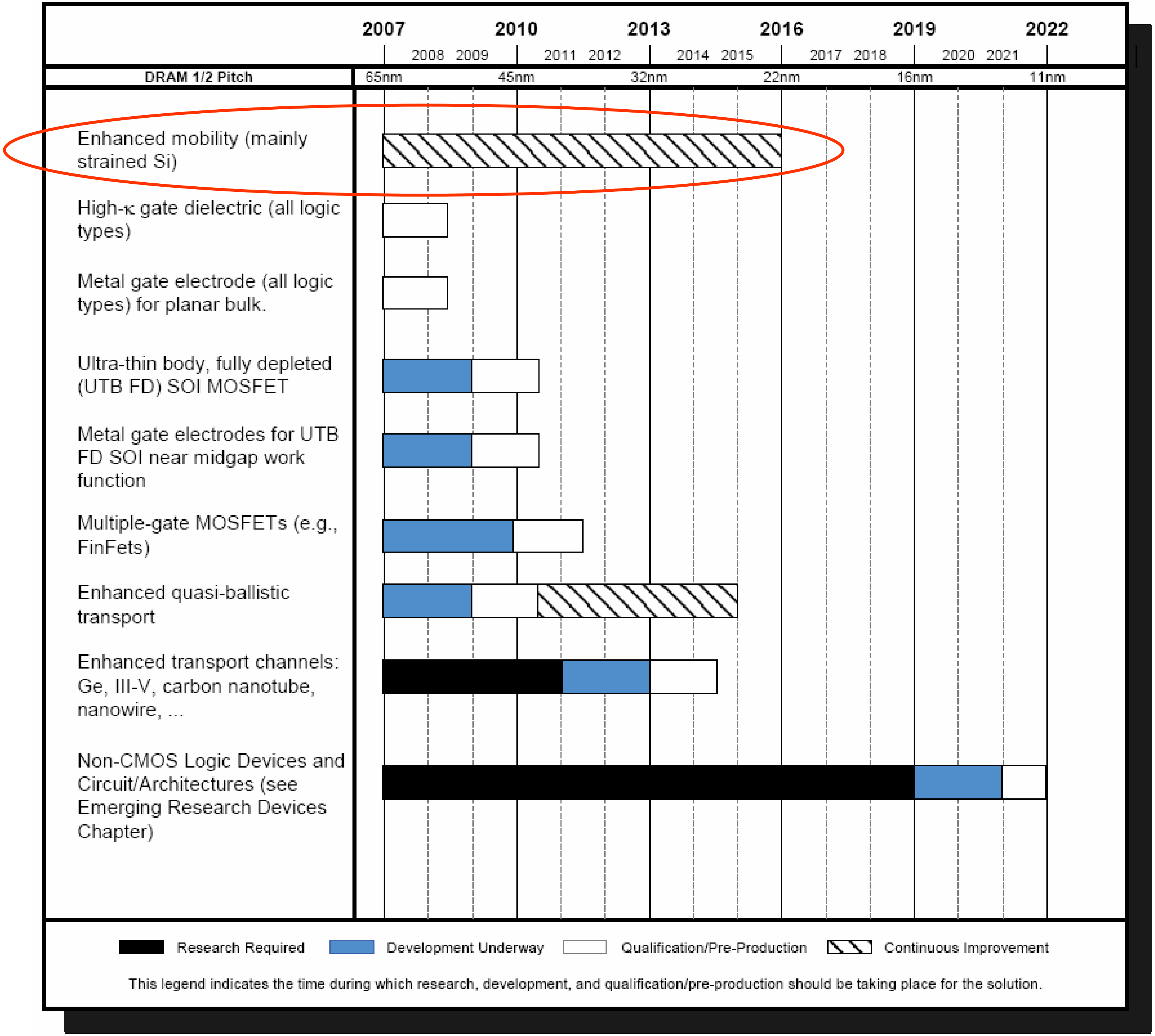
Overview (Top-view)



Zoom-in (3D-view)



G. S. Kar, S. Kiravittaya, U. Denker, B.Y. Nguyen, and O. G. Schmidt, Appl. Phys. Lett. 88, 253108 (2006)



Source: ITRS 2007

„A method of making a semiconductor device having an arched structure strained semiconductor layer“

B.-Y. Nguyen, S. G. Thomas, A. Wild, P. Wennekers, L. Cergel, T. White, A. Thean, M. Sadaka
Freescale Semiconductor Inc.
D. Grützmacher
Paul-Scherrer-Institut, CH5232, Switzerland
O. G. Schmidt
Max-Planck-Institut für Festkörperforschung, Heisenbergstr. 1, D-70569 Stuttgart

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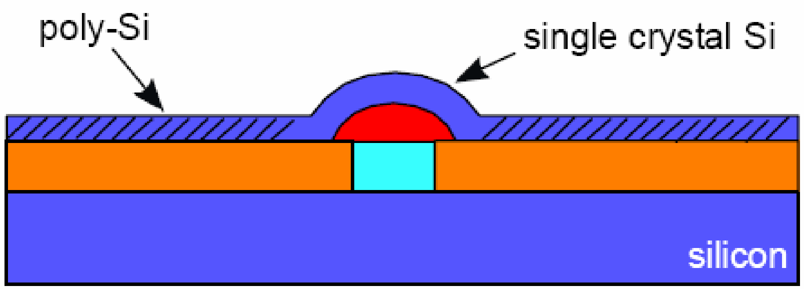
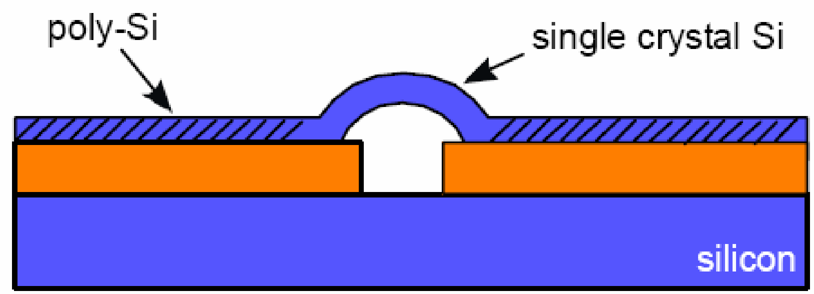
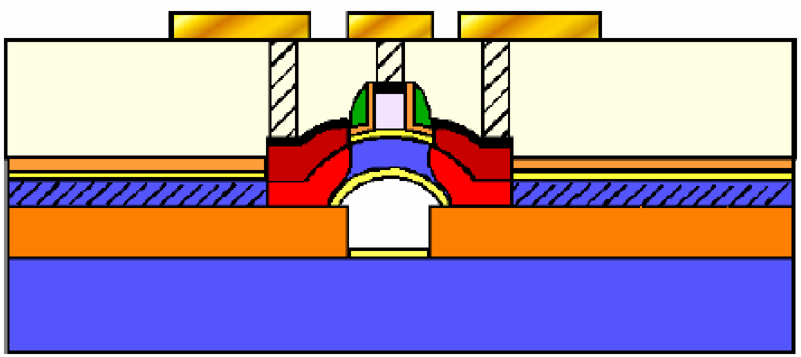
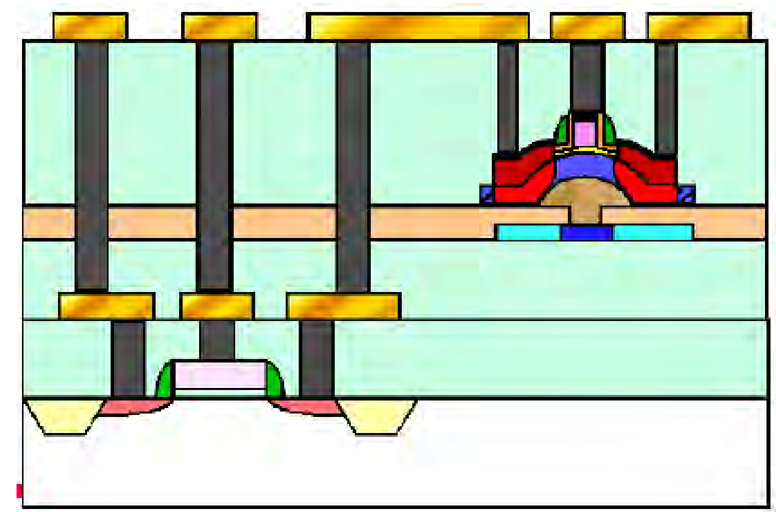


4. Overgrow Ge dot with Si



5. Selective etch of Ge dot and Si/SiGe seed





US Patentanmeldungen: 11/093,645
11/094,008

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PHYSICA E
Physica E 25 (2004) 280–287
www.elsevier.com/locate/physe

Novel nanostructure architectures

O.G. Schmidt[a,*], A. Rastelli[a], G.S. Kar[a], R. Songmuang[a], S. Kiravittaya[a], M. Stoffel[a], U. Denker[a], S. Stufler[b], A. Zrenner[b], D. Grützmacher[c], B.-Y. Nguyen[d], P. Wennekers[e]

[a] *Max-Planck-Institut für Festkörperforschung, Heisenbergstrasse 1, D-70569 Stuttgart, Germany*
[b] *Universität Paderborn, Experimentalphysik, Warburgerstr. 100, D-33098 Paderborn, Germany*
[c] *Paul-Scherrer-Institut, CH-5232, Switzerland*
[d] *Advanced Products R&D Laboratory, Motorola incorporated, 3501 Ed Bluestein Boulevard, Austin, TX 78721, USA*
[e] *Digital DNA Laboratories—EMEA, Motorola incorporated, Am Borsigturm 130, D-13507, Berlin, Germany*

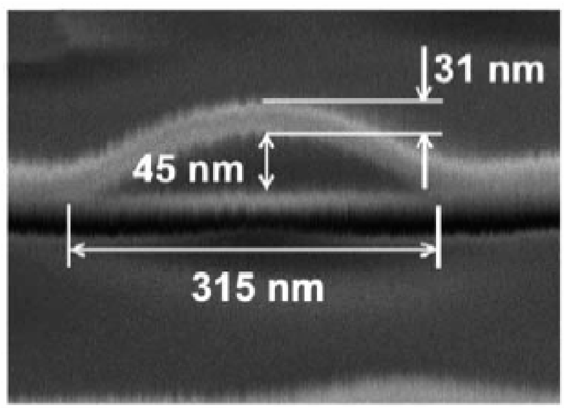

Fig. 7. Fabrication of ultra-thin free-standing Si bridges. (a) Schematic illustration of the required processing steps: Mesa definition on surface with Si-capped SiGe islands and subsequent selective etching of the SiGe core results in free-standing Si bridges. (b–d) Different views of the fabricated Si bridges.

Conclusion

- Further transistor scaling requires rigorous increase of strain in channel

- SiGe island growth is well-understood and could help to establish sufficient strain down to 22nm technology