Landscape of materials design for future nano electronics and high-throughput materials exploration

(Toyohiro Chikyo)

Abstract :

T.Chikyow[1,], T.Nagata[1], N.Umezawa[1], M.Yoshitake[1],K.Ohmori,[3], T.Yamada[3], H. Watanabe[4] , K.Shiraiishi [5] and H. Koinuma[1, 2]

[1] *National Institute for Materials Science (NIMS), Tsukuba, Ibaraki 305-0044, Japan*

[2] *Japan Science and Technology Agency (JST),Chiyoda-ku Tokyo 102-0084, Japan*

[3] *Nano Technology Research Laboratory (NRL) Waseda University, Shinjuku-ku, Japan*

[4] *Osaka University, Suita Osaka 565-0871, JAPAN*

[5]*Tsukuba University, Tenno-dai, Tsukuba Ibaraki 305-8571, JAPAN*

In the modern large scale integrated circuit (LSI), due to the scaling of the MOSFET, selection and design of the gate stack materials have been the most serious problem. At this moment, for the gate oxide, HfO_2 based oxides are expected to be the candidate but materials exploration for the next generation has already started. For example La based high-k materials are discussed as the candidate.

For the gate materials, the work function tuning of gate materials for nMOS and pMOS are required to make CMOS structure. However, the Fermi level pinning at the metal gate/ high-k oxide interface becomes a serious barrier because the pinning effect affects the controllability of the work function. Shiraishi et al showed a model to explain the pinning phenomena from the metal/oxide reaction and Akasaka et al demonstrated to control the pinning with different thickness of the gate oxides based on the Shiraishi model.To investigate the origin of the Fermi level pinning, quite recently Toriumi et al proposed another model that the Fermi level pinning was caused only by the interface dipole between high-k oxide and underlying SiO_2 grown on Si substrate. This model was experimentally demonstrated by Ota et al.

To make clear the origin of the Fermi level pinning and to show the strategy for control the Vth in CMOS, more detailed and well designed experiments are required for the suitable materials design. Also these experimental results can be applied to the future nano electronics device where we must fabricate fine surrounding gate on the Si nano wire instead of the planner processed devices. Here again the new materials exploration will play a major role in nano electronics. The key issue, however, is the speed for the exploration.

It has passed more than 10 years since the modern combinatorial materials science appeared with new tools for high throughput characterizations. Recently this combinatorial methodology is recognized to be an innovative tool to screen a lot of materials in a short term and to discover new materials. The striking advantage of this method is that we can get a systematic data where composition or film thickness is changed linearly. This data help us to understand how the property changes according to the composition or film thickness. Expectation for this method is potentially increasing

In this talk, we show some examples which combinatorial materials exploration gives a landscape of the new materials design for the future nano electronics.