

On the control of GeO₂/Ge and metal/Ge interfaces toward metal source/drain Ge CMOS

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Abstract :

In order to realize high performance devices of Ge beyond Si, it is required to control two interfaces of Ge. One is Ge/dielectric interface and the other is Ge/metal one. It is quite important to form a stable GeO₂ interface beneath the high-k dielectrics on Ge. Concerning the Ge/metal interface, we have demonstrated that any metals/p-Ge junctions are ohmic, while any metals/n-Ge ones show Schottky behavior, due to the strong Fermi-level pinning (FLP) near the valence band edge of Ge [1].

In this paper, we discuss how to stabilize the GeO₂/Ge interface and how to unpin the strong FLP at metal/Ge interface.

Experiments on the volatility of GeO₂ films have indicated that a lack of thermal robustness of GeO₂ comes from the volatile GeO formation through the reaction of GeO₂ with Ge, and that the volatilization of GeO from the interface should be the origin of the interface deterioration in GeO₂/Ge MIS capacitors. To solve this problem, we performed the thermal treatment after capping the gate electrode on GeO₂/Ge. A dramatic improvement of GeO₂/Ge interface has been achieved.

As for the strong FLP at metal/Ge, the *metal-induced gap states* (MIGS) might be a plausible origin [1]. The MIGS is basically due to the metal wave function tailing into Ge gap states. So, in order to relax the FLP, it would be effective to protect the metal wave function penetration into Ge, namely to insert an insulator layer between metal and Ge. J-V characteristics of Au/n-Ge *with* and *without* the ultra-thin insulator have shown a distinct transition from Schottky to ohmic characteristics on n-Ge.

Two methods controlling both interfaces have enabled us to make the metal source/drain Ge n-MOSFETs for the first time [2] as well as p-MOSFETs.

[1] T. Nishimura, K. Kita, A. Toriumi, Appl. Phys. Lett. **91** (2007) 123123.

[2] T. Takahashi, T. Nishimura, L. Chen, S. Sakata, K. Kita and A. Toriumi, IEDM (2007).