JST-MOST Workshop
on "Nanoelectronics and System Integration for AI"

Date 10 a.m. – 5 p.m. 14th June, 2019 *Registration starts on 9:45.

Venue 1st Meeting room and Hall, 2nd floor, Campus plaza Kyoto
939 Higashi-Shiokoji-cho, Nishinotoin-dori and Shiokoji sagaru, Shimogyo-ku, Kyoto-shi

Workshop program

9:55 **Photo at 1st Meeting room**

10:00—10:05 **Opening remark**

Ms. Yoshiko Shirokizawa

Executive Director, Japan Science and Technology Agency

10:05—10:10 **Introductory remark**

Dr. Toshihiko Kanayama

WS coordinator

Special Emeritus Advisor, National Institute of Advanced Industrial Science and Technology

Visionary talk

10:10—10:40 (25min + QA 5min)

Nanoelectronics and System Integration for the Future

Prof. Takayasu Sakurai

Professor, Department of Technology, The University of Tokyo

10:40—11:10 (25min + QA 5min)

Neuromorphic Dynamics towards Symbiotic Society with AI/Robots

Prof. Minoru Asada

Specially Appointed Professor, SISReC, Institute for Open and Transdisciplinary Research Initiatives, Osaka University

11:10—11:40 (25min + QA 5min)

Semiconductor Moonshot Project in Taiwan

Prof. Tai-Cheng Lee

Professor, Department of Electrical Engineering, National Taiwan University

11:40－12:10 (25min + QA 5min)

Challenges and Activities for AI Edge Computing in Taiwan's Microelectronics Program

Prof. Meng-Fan Chang

1. Program Director, Microelectronics Program, MOST 2. Professor, National Tsing Hua University 3. President, IEEE Taipei Section

12:10-13：10 **Lunch at Hall** *Please put your poster on board

Contributed presentation

13：10-14：30 **at 1st Meeting room**

P-01 AIAugSurgery: Image-guided Surgery Navigation System

Prof. Chia-Hsiang Yang

Professor, Department of Electrical Engineering, National Taiwan University

There have been many augmented reality (AR) smart glasses, such as Microsoft HoloLens, but there is no existing system with 3D dynamic information augmentation for real-time surgery applications. In this project, we are developing an AR surgery assistance system with artificial intelligence (AI). The proposed AR system can automatically display the locations of blood vessels, nerves, and lesions in real-time to meet potential clinical and training needs for surgery. We are building the system by jointly considering algorithm, architecture, and circuit parameters. Algorithms for constructing 3D organ models, augmented medical images, and augmented endoscope images have been developed. As for portable devices, an energy-efficient AI engine for convolutional neural network acceleration with low-voltage circuitry are being developed. Technical breakthroughs also include data augmentation for semantic segmentation, neural network training for endoscope images, neural-network based pose estimation, and adaptation for 3D human models.

P-02 Artificial Intelligent 3D Sensing Image Processing System for Array Sensing Lidar

Prof. Chao-Tsung Huang

Associate Professor, Department of Electrical Engineering, National Tsing Hua University

This project aims to develop an inside-out 3D scene reconstruction system with great depth precision, long depth range, high noise resistance, and high-definite image resolution for immersive augmented/virtual reality (AR/VR) applications. It consists of three sub-systems for processing light, electrons, and digital signals sequentially. The first one is an active depth sensing system which integrates an pulsed chaotic lidar transceiver and an array avalanche

photodiode (APD) light sensor. The former can outperform infrared sensing in terms of distance range (up to 20 meters) and depth precision, and the latter enables high sensitivity and multi-pixel sensing. In addition, the lidar system adopts eye-safe laser for enabling daily use. Our second sub-system is comprised of time-of-flight demodulation circuits for smart 3D sensing and a depth image processor with artificial-intelligence (AI) noise reduction capability. The last sub-system is an embedded convolutional neural network (CNN) processor to provide high-performance AI acceleration. For example, it can generate high-precision and high-resolution depth images by fusing low-resolution ones with RGB images.

This project jointly considers circuit design, lidar system, AI algorithm, and CNN accelerator to optimize the overall performance. It will overcome the physical limitation of light by using array APD sensor, chaotic lidar, and AI-based noise control to increase depth precision, distance range, and field of view. We also plan to build up an AI-edge computing platform to accelerate AI-based 3D sensing and image recognition. Finally, we hope that this system will enable great AR/VR experience through array sensing lidar and AI-edge computing.

P-03 Enabling Technology of Object Recognition and Tracking for Mobile Devices – Towards a Neuromorphic Intelligent Vision System

Prof. Kea-Tiong Tang
Professor, Department of Electrical Engineering, National Tsing Hua University

Deep neural network is currently applied to various artificial intelligence tasks including computer vision, speech recognition and robotics. Visual signal processing is a crucial aspect of artificial intelligence. Although deep neural network provides very high accuracy to process visual information, the massive model causes extremely high computing power consumption and is difficult to implement in mobile devices. This project aims to solve this crucial problem by integrating biological principle and neuromorphic architecture with deep neural network to develop a neuromorphic intelligent visual system-on-chip for mobile devices. The project includes four aspects: 1) low-power intelligent visual image sensing chip, 2) neuromorphic neural network chip for analog sensing of insect vision and spatial recognition, 3) realization of a low-latency and low-power deep learning chip based on neuromorphic intelligence, 4)an analog-digital mixed neuromorphic intelligent chip architecture. By integrating these four subprojects, we aim to design, develop, and integrate a low-voltage, low-power, realtime mobile neuromorphic intelligent visual system that can perform tasks of recognition and track prediction.

P-04 Verification platforms for AI integrated chip technology and application

Dr. Kai-Shin Li

Research fellow, Taiwan Semiconductor Research Institute, National Applied Research Laboratories

Dr. Fu-Kuo Hsueh

Associate engineering, Taiwan Semiconductor Research Institute, National Applied Research Laboratories

In the near future, a variety of electronic information products could be connected in the piece through the high speed network to provide on the daily lives of human convenience, and even change the behavior of people's lives. And this is what we call as internet of things (IOT) or artificial intelligent (AI) application. In AI device, huge data must have a corresponding information processing media to use as computing and data storage, the most representative techniques is the memory processor (Process-in-Memory; PIM). We believe PIM technology will become the key in AI and big data analysis.

Taiwan Semiconductor Research Institute (TSRI) provides several verification platform, form device fabrication to chip package, to support and develop on AI-chip integration and application. 1. SOC-high speed, Fatigue-Free, Low power emerging memory: advance facilities, ultra-thin metal or metal oxide film deposited system and atomic layer etching system, set up for< 50 ns memory array chip integration with M3 process. 2. SOP-3D heterogeneously integrated chip: through Interposer and TSV technology, the various function chips can be packaged together to create new application for Ai. 3. Industrial virtual nano laboratory: New material study and new device fabrication supported in TSRI help industries look for the next generation technology path on AI. 4. AI-creative Laboratory: User can develop their own algorithm and simulate chip function on TSRI computing system. 5. Silicon Photonic and quantum communication laboratory: TSRI provides EIC design, Synopsys, Cadence and Mentor graphic training and technical support on big data communication. 6. AI-edge on 3D computing memory: Monolithic 3D technology integrate the new emerging memory to realize and verify logic computing in memory. 7. AI-edge emerging memory: TSRI also develops several different kind of non-volatile memory, PC-RAM, MRAM, RRAM and FEFET for user designing the high speed and low power computing chip.

P-05 FinFET Thermal Modeling and Circuit Thermal Simulation

Prof. Chee Wee Liu
Distinguished/Chair Professor, Electrical Engineering, National Taiwan University

Mr. Chia-Che Chung
Ph.D. student, Department of Electrical Engineering, National Taiwan University

A physics-based thermal SPICE model of FinFET considering the boundary scattering, alloy scattering, and frequency-dependent transient response is proposed. The continuous device scaling leads to the increasing boundary scattering, and the introduction of SiGe S/D in pFETs results in alloy scattering. The proposed SPICE model is verified by the TCAD simulation. Furthermore, the distributed interfacial thermal resistance is added into the SPICE model. The interfacial thermal resistance is resulted from the phonon mismatch between different materials, leading to a temperature difference across the interface. Considering the interfacial thermal resistance causes an additional 42℃ rise in junction temperature. In addition, the thermal behavior of BEOL is characterized by the two-step pseudo isothermal plane. Both R_{th} and C_{th} elements of the BEOL thermal model are validated by the TCAD simulation as well. This comprehensive thermal SPICE model of the FinFET and BEOL is applied for the self-heating simulation of the inverter and ring oscillator to obtain the circuit-level temperature distribution and reliability prediction. The BEOL materials, via 2 bundle pitch, and number of vias are demonstrated to be important knobs for self-heating aware circuit design.

P-06 Platform of Ge finFETs

Dr. Yao-Jen Lee
Research fellow, Taiwan Semiconductor Research Institute, National Applied Research Laboratories

Ge is attractive for the future technology nodes. However, the Ge MOSFET technology is facing several serious challenges, including fast n-type dopant diffusion, high junction leakage, EOT scaling, Dit reduction and enormous dislocation defects in the Ge epi-layer on Si substrates because of the large lattice mismatch to Si. In addition, a high-quality, fine-controlled, atomic-thin interfacial layer (IL) between the Ge channel and high-k gate dielectric is crucial for EOT scaling and device performance, but remain challenging because of the unstable IL of germanium oxide and decomposition of several germanium suboxides (Ge_yO_x). The damages induced by fin dry etching on the three-dimensional (3D) sidewalls was also reported to degrade the interface quality. In this study, the Ge FinFET CMOS inverters were successfully demonstrated by newly introduced combination processes of MWA and in-situ ALD digital O3 treatment. The superior SS characteristics with high I_{ON}/I_{OFF} ratio were achieved for Ge n- and

p-FinFETs, respectively. The Ge CMOS inverter shows the high voltage gain of 50.3 V/V thanks to the interface states reduction caused by the in-situ ALD digital O_3, indicating the potential of Ge for CMOS applications in advanced technology nodes.

P-07 Ion implantation after germanidation: low thermal budget S/D fabrication method for Ge/GeOI devices towards monolithic 3D integrations

Dr. WENHSIN CHANG
Researcher, National Institute of Advanced Industrial Science and Technology

Ion implantation after germanidation (IAG) technique has been implemented for low thermal budget bulk Ge and UTB-GeOI n- and p-MOSFETs. Dopant segregation at NiGe/Ge interface by low temperature drive-in annealing has an advantage in forming an abrupt metallic source/drain (S/D) junction, which is not only effective for bulk Ge but also for UTB-GeOI substrate. IAG technique is proved to be a low thermal budget process for both Ge n- and p-MOSFETs with a high I_{on}-I_{off} ratio and low parasitic resistance, which is also benefit for future monolithic 3D integrations.

P-08 Cluster-Preforming-Deposited Si-rich W Silicide: A New Contact Material in CMOS for Edge AI Systems

Dr. Naoya Okada
Researcher, National Institute of Advanced Industrial Science and Technology

Edge AI systems require low-power operations as well as high performance. Accordingly, CMOS circuits need transistors that ensure enough on-state current while decreasing the off-state leakage. The source/drain (S/D) resistance reduction without depending on extreme doping is therefore essential; i.e., low Schottky barrier height (SBH) at the metal/semiconductor interface is required to reduce the contact resistance at S/D. In this work, we demonstrate a novel contact material with low SBH of 0.32 eV for n-FET: the WSi_n (n = 12) composed of W-atom-encapsulated Si_n cage clusters. The WSi_n film was prepared by the newly developed Cluster-Preforming Deposition (CPD) method. Furthermore, this film exhibited excellent diffusion barrier properties for Cu and Co contacts: a high barrier stability against annealing up to 600−700 °C. Consequently, this film is a promising contact material in CMOS for edge AI systems.

P-09 Ferroelectric HfO_2-based transistor and memory for energy efficient computing in IoT edge device

Prof. Masaharu Kobayashi
Associate professor, Institute of Industrial Science, The University of Tokyo

In today's highly information-oriented society, more and more electronic devices are needed for high-end servers in cloud and sensor node devices in edge. Because of the power constraint, highly energy-efficient computing is required, which is enabled by new transistor and memory technologies. For energy-efficient computing, higher I_{on}-I_{off} ratio at lower supply voltage can be obtained by using steep subthreshold slope (SS) transistor, and normally-off operation can be performed by using low-latency/low-power non-volatile memory. Those logic and memory technologies must be developed at low cost. Recent discovery of ferroelectric (FE) HfO_2 enables low-cost and energy-efficient logic and memory devices.

In this talk, our recent research progresses on ferroelectric FET (FeFET), non-volatile SRAM (NV-SRAM), and FE tunnel junction memory (FTJ), all of which are based on FE-HfO_2, will be overviewed. Particular topics will be: (1) device physics in steep subthreshold behavior of FeFET, (2) opportunity of NVSRAM in the context of IoT, (3) device design and scaling prediction of FTJ.

P-10 Material and Device Design Studies in Ferroelectric-Gate FETs for AI Applications

Dr. Shutaro Asanuma
Senior Scientist, National Institute of Advanced Industrial Science and Technology

Dr. Shinji Migita
Researcher, National Institute of Advanced Industrial Science and Technology

Integration of both memory and logic functions in individual devices on LSI is an attractive way to produce excellent AI systems that combine high-efficiency and low-power consumption. Ferroelectric-gate FETs (FE-FETs) have a potential to realize such devices. In AIST, we are working with the development of HfO_2-base ferroelectric films and fabrication of FE-FETs.

It is well known that ferroelectric properties of HfO_2-based films change sensitively with the dopant concentration in the films. We found that it is caused by the kinetics of crystal phase transformation where dopants in the films suppress the reaction rate. Based on this understanding, we are now challenging to the modulation of ferroelectric properties of HfO_2 films.

In the operation of FE-FETs, a major concern is the charge balance between the ferroelectric capacitor and the channel capacitor of FET. Ferroelectric polarization charges are usually very large, and easily induce the breakdown of dielectric films in FETs. Therefore, design of capacitors in FE-FETs is directly linked with their performances. Improvement of the fabrication process is

ongoing.

We consider that following two issues are critical for the utilization of FE-FETs in AI applications. One is the analogue-mode operation, and the other is the low-voltage operation. In order to construct these technologies on FE-FETs, we are focusing to design both the ferroelectric materials and the device structures at nanometer-scale-conscious.

P-11 Device simulator for exotic materials and its application to negative capacitance FET

Dr. Tsutomu Ikegami
Researcher, The National Institute of Advanced Industrial Science and Technology

A new device simulator named Impulse TCAD was developed. Impulse TCAD is built on top of a nonlinear finite volume method solver, which is further based on the Python script language and its associated scientific libraries. Users can fully customize device properties and/or equations from the run scripts, which allows ready handling of exotic materials with non-standard physical models. As a demonstration, transient analysis of the negative capacitance field effect transistors (NC FET) is performed. A ferroelectric material in NC FET is handled by the time dependent Ginzburg-Landau-Devonshire (GLD) equation, while the standard device equations are applied on the rest of the device. The simulations show that starting from the spontaneous polarization state, the ferroelectric regions evolve into the negative capacitance regime, showing expected characteristics as NC FET. They also indicate that the Ginzburg term in the GLD equation, which is related to the correlation radius, plays an important role for the negative capacitance effect to be revealed. When the correlation radius is too small compared to the channel length, the ferroelectric region is segregated into multiple polarization domains, losing the NC FET characteristics.

P-12 High-precisely and Defect-free Gate Etching of GaN HEMT Device for Realizing High-Speed mm-Wave Communication

Dr. Daisuke Ohori
Postdoctoral fellow, Institute of Fluid Science, Tohoku University

The amount of information in the network is becoming larger and larger with the development of the Internet of Things (IoT) society. Wireless high-speed data transfer technology is very important for processing big data with AI. In order to realize high-speed big data communication, mm-wave communication technology by GaN HEMT device attracts much attention. However, the performance of GaN HEMT devices is degraded due to normally on and current collapse. In order to solve these problems, we need to improve the gate etching process. Fluorine gas plasma leads to higher sheet resistivity under the gate electrode and generates defect in the GaN by UV irradiation. In this study, I demonstrated the way to improve GaN HEMT performance

by defect-free atomic-layer etching with Cl_2 neutral beam (NB) etching.

The SiN layer etching on the GaN HEMT sample was needed for fabricating the gate electrode. The NB system installed aspect-ratio carbon aperture plate neutralizes the ions in the plasma varying the kinetic energy of ions by applying RF bias power and prevents the UV photon irradiation. I controlled weakly the kinetic energy of ions to the sample surface by controlling the RF bias power at 10 W. As a result, SiN and GaN etching rate was 1.1 and 0.6 nm/min, respectively. The atomically controlled etching was controlled. The sheet resistance was 380 ohm/square that was the same value before etching the GaN surface. For the results of Schottky characteristic measurement, n value for chlorine neutral beam and CF_4 plasma was 1.44 and 1.62, respectively. Moreover, for the current collapse characteristic, the current reducing did not occur. Therefore, we succeeded in the fabrication of good performance GaN HEMT device based on the gate etching process with the neutral beam. The defect-free and atomically controlled etching by the neutral beam is very important for fabricating the high-performance GaN HEMT device.

P-13 Tensile-strained GeSn-on-SOI MSM Photodetector Fabricated by Solid-phase Epitaxy

Dr. Hiroshi Oka

Researcher, National Institute of Advanced Industrial Science and Technology

Group-IV Germanium-tin (GeSn) alloy has attracted a great interest for near- and mid-infrared sensing devices due to its tunable band structure depending on Sn content and strain. In this study, we have demonstrated GeSn metal-semiconductor-metal (MSM) photodiode array fabricated on Si-on-insulator (SOI) substrate by using solid-phase epitaxy method. A tensile-strained GeSn thin film was directly grown on Si layer by performing rapid thermal annealing for amorphous-GeSn/SOI structure. A photoluminescence (PL) emission from solid-phase-grown GeSn layer was red-shifted and the peak wavelength reached 1800 nm, indicating bandgap shrinkage by Sn incorporation (5%) and tensile strain (0.2%). A GeSn MSM photodiode array fabricated on SOI substrate exhibited clear optical response to infrared illumination thanks to its high-crystallinity. This technology will facilitate the integration of mid-infrared sensing devices and integrated circuits on a Si chip.

P-14 Highly Sensitive Terahertz Wave Arrayed Sensor Implemented by Using Semiconductor on Glass Technology

Dr. Takeshi Kuboki
Assistant Professor, Kyushu University

Prof. Tanemasa Asano
Professor, Kyushu University

Utilization of terahertz waves, near 1 THz band in particular, remains as a technical challenge for future functional sensing and communication. Developments of high-power wave emitter and high-sensitive wave detector are mandatory. We have developed the terahertz wave detector whose noise equivalent power is as small as 1 pW/Hz$^{1/2}$ at 1.0 THz. The detector was fabricated using HEMT on glass structure which was implemented by using the layer transfer technology. We have also develop a circuit model of the detector, which can well explain the relation between observed sensitivity and device parameters such as the subthreshold slope, channel mobility, and channel length.

P-15 Switching and synaptic behavior of neutral oxygen irradiated-ZnO transparent memristor

Dr. Firman Mangasa Simanjuntak
Research Associate, WPI-Advanced Institute for Materials Research, Tohoku University

Transparent memristor is expected to have an essential position in the fabrication and the realization of invisible, wearable, and smart electronics due to its potential for future nonvolatile memory and neuromorphic computing applications.[1] Memristor devices having analog switching behavior can be programmed to mimic a biological synapse; synapse is one part of the neuronal system that controls the transfer of information from one neuron to the other.[2]

ZnO is an excellent material for fabricating invisible electronics due to its high transparency. However, the abundance of native defects hinders the realization of high-performance ZnO-based memristor devices.[3] Various method has been proposed to mitigate this issue; yet, the proposed methods are time-consuming and some of them are not designed for use in invisible AI on-chip high-density hardware.[3–6] In this work, we develop high performance pure and thin ZnO-based transparent memristor devices showing synaptic behavior by employing neutral oxygen irradiation; the low kinetic energy of the neutral oxygen ions beam is beneficial to avoid surface/etching damage.[7]

Reference
[1] F.M. Simanjuntak, D. Panda, K. Wei, and T. Tseng, Nanoscale Research Letters **11**, 368 (2016).
[2] F.M. Simanjuntak, S. Chandrasekaran, C. Lin, and T.-Y. Tseng, APL Materials **7**, 051108 (2019).
[3] F.M. Simanjuntak, D. Panda, T.-L. Tsai, C.-A. Lin, K.-H. Wei, and T.-Y. Tseng, Applied Physics Letters **107**, 033505 (2015).
[4] F.M. Simanjuntak, O.K. Prasad, D. Panda, C.-A. Lin, T.-L. Tsai, K.-H. Wei, and T.-Y. Tseng, Applied Physics Letters **108**, 183506 (2016).
[5] F.M. Simanjuntak, S. Chandrasekaran, B. Pattanayak, C.-C. Lin, and T.-Y. Tseng, Nanotechnology **28**, 38LT02 (2017).
[6] F.M. Simanjuntak, S. Chandrasekaran, C.-C. Lin, and T.-Y. Tseng, Nanoscale Research Letters **13**, 327 (2018).
[7] F.M. Simanjuntak, T. Ohno, and S. Samukawa, ACS Applied Electronic Materials **1**, 18 (2019).

P-16 A Growing Polymer-Wire Neural Network in Electrolysis Solution

Dr. Megumi Akai-Kasaya
Assistant professor, Osaka University

Brain-inspired neuromorphic computing that fuse memory and parallelly proceed should offer significant energy savings as similar as the brain works. Custom-designed neuromorphic hardware specialized for an artificial neural network using emerging material memory devices is now actively developed. A future of which various stage of neuromorphic hardware is widely used in edge technologies is a clear and present demand of society. Appearance of new synaptic devices consisting of organic material with unique benefits has recently been reported, though no neural network learning were performed yet. We here present a prototype of neural network consisting of a conducting polymer. The conducting polymer grows in wire shape between electrodes immersed in monomer solution increasing its conductance, which can be stiffly kept as a resistance change memory. We use PEDOT:PSS [poly (3, 4-ethylenedioxy-thiophene) doped with poly (styrene sulfonate) anions], which attracts a great attention because of its wide variety of functions, i.e., high conductivity, high chemical sensitivity, bio-adaptability, transparency, flexibility and high environmental durability. We successfully accomplished a learning of an autoencoder neural network consisting of PEDOT:PSS wires, which realizes feature extraction of three 3×3 binary letters encoding from high dimensional 9-pixel to low 3-pixel information. The polymer resistance array can be mounted in versatile hardware applications that need desired combination of resistive weight. The realization of machine learning of the resistive weight of conducting polymer broadens variety of material and framework to realize physical neural network.

P-17 Development of quantum dot solar cells for IoT power units

Dr. Susumu Toko
Assistant Professor, Tohoku University

In recent years, the world has focused on Internet of Things (IoT) including AI edge technology. One of the most important issue for IoT is energy consumption. For improving energy efficiency, development of the device with low energy consumption is an approach, but development of the power unit for IoT is also an important approach, what is called energy harvesting technology.

Quantum dot solar cells (QDSC) is a hopeful device for IoT power unit. It can handle a wide range of wavelengths such as not only solar light but also fluorescent light, even if that film thickness is thin. IoT requires thin film because flexibility is the most important factor for ubiquitous sensors.

The determining the absorption wavelength in QDSC is quantum dot super lattice (QDSL) structure, but ideal QDSL is very difficult to fabricate for current nanotechnologies. Conventional technologies, such as chemical solution methods and molecular beam epitaxy (MBE), can fabricate relatively uniform quantum dots (QDs). However, very few technologies can finitely arrange QDs to form a quasi-crystal structure. The conventional bottom-up process with MBE technology can achieve only very limited control along the growth direction.

Recently, we fabricated high quality QDSL with high density and regular array by combining with damage-free neutral beam etching (NBE) and self-assembled biotemplate, which is the advanced top-down nanofabrication process.

Here, we report the results of fabricating high quality quantum dot solar cells as IoT power units utilizing NB.

Poster session

14：30-16：00　at Hall

Poster session & *like*

i) Most interesting ・vote by ALL participants, 3 votes/person **ii) Joint research** ・vote by Visionary talker and Contributed Presenter, 3 votes/person

like: vote for each other and put stickers on the sticker chart.

16:00-16:10　Break & withdrawal of poster

16:10　Photo at Hall

Closing session

16:10-16:30　Closing session (includes Wrap-up discussion)

Vote: You may vote as many as you like.

Promising theme
1) Innovative AI computing technologies
2) Intelligent sensing and communication technologies
3) Innovative building technology for AI devices and systems
4) Non-traditional applications of edge AI and IoT
5) Others, if any

16:30-16:35　Closing remark

Prof. Bing-Yu Chen

Professor, Department of Information Management, College of Management, National Taiwan University

Networking party

17:00-　Opening remark

Dr. Jiun-Rong Chen

Director, Science and Technology Division, Taipei Economic and Cultural Representative Office in Japan

18:00-　Closing remark

Ms. Yoshiko Shirokizawa

Executive Director, Japan Science and Technology Agency