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Research Topics about solution derived PZT

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I will introduce research topics related solution based PZT, which have been conducted in JST-ERATO Shimoda nano-liquid process project from October 2006 to March 2012. ERATO, Exploratory Research for Advanced Technology, is one of major research funding programs provided by Japan Science and Technology Agency (JST).

The research objective of ERATO Shimoda project is to create a new method to print nano-sized authentic electronics devices and circuits using functional solutions. As one of the target devices, we chose FGT (Ferroelectric Gate Transistor). As for a structure of FGT, a bottom gate one, in which ITO and PZT were a channel and gate insulator layer, respectively, was adopted. The polarization of PZT is so large that it can completely deplete the ITO channel. So, this structure can be a transistor with memory function caused by the hysteresis of PZT. Three topics will be introduced: (1) low temperature formation of PZT by using chemical solution deposition (CSD) methods, (2) totally solution processed FGT and (3) a NAND memory constructed by solution processed FGTs.

(1) low temperature formation of PZT We found a novel low-temperature crystallization path where the perovskite structure were directly formed at 400 -500 degree C without passing through pyrochlore formation. This is caused by the reaction that reductive agents such as monoethanolamin or curbon reduce Pb^{2+} to Pb^{0} at 200-300 degree C so that there is no way for pyrochlore phase can be formed due to the shortage of Pb element.

(2) totally solution processed FGT Prior to direct printing of FGT, it should be fabricated only by using solution materials . By adopting LaNiO for a gate and ITO both for a channel and source/drain electrodes, a FGT with high performance was developed. Its all layers were constructed by metal-oxide materials which were made from solution precursors.

(3) NAND memory A new circuit design was invented to make a NAND circuit using FGT as a memory element. The developed NAND circuit has dual FGT cells, one of which is for a memory while the other is a pass transistor. Non-destructive writing, reading and erasing operations were demonstrated without any disturbance.