Single-Grain Si TFTs using Spin-Coated Liquid-Silicon

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Abstract

Liquid silicon material, which is a solution of CPS in organic solvent, offers us an opportunity of fabricating TFTs using spin-coated or printed silicon, instead of traditional organic materials. In our investigation, we have fabricated single-grain Si TFTs on location-controlled Si grains with laser crystallization of a-Si formed from spin-coated liquid Si. Si grains with maximum grain diameter over 3um were positioned at predetermined sites. Mobilities for electrons and holes are 391 cm2/Vs and 111 cm2/Vs, respectively.

Introduction

In the flexible electronics, printing is attractive as it realizes a non-vacuum and non-photolithography process hence a low-cost manufacturing. Printed organic semiconductor TFTs have been investigated extensively, however the carrier mobility and reliability are much inferior in comparison with silicon devices. New material, liquid silicon, which is a hydrogenated polysilane in an organic solvent, offers us a chance to print silicon devices on a flexible substrate. Shimoda, et al. [1] succeeded in fabricating polycrystalline Si TFTs with laser crystallization of amorphous-Si precursor formed from the liquid-Si. However the performance is limited by the grain boundaries in the channel because of the randomly positioned poly-Si grains. If the location of the grains can be controlled, TFTs could be fabricated inside the grain and performance would reach the crystalline-Si counterpart. This will realize high-speed circuits in the flexible electronics and may alter the fabrication process in ULSI.

In this paper, we fabricated single-grain (SG) Si TFTs in location-controlled Si grains, which are formed with laser crystallization of a-Si using spin-coated liquid-Si. We have succeeded to form grains with a diameter of 2 um at predetermined positions, and the carrier mobilities of the single-grain Si TFTs are 391 cm2/Vs and 111 cm2/Vs for the electrons and holes, respectively.

Experiment

We used the micro-Czochralski process [2] to control the position of Si grains. Figure 1 shows a schematic view illustrating the fabrication process. First, a grid of 100nm wide and 700nm deep holes (grain-filter) have been formed in 1.6 micron thick SiO2 on a crystalline Si substrate. 21-wt% solution of UV-irradiated CPS (liquid Si) was then spin-coated on the structure at a rotation speed of 2000 rpm and baked at 430oC for 60 min to remove the solvent and to form a-Si. The film thickness was 112 nm. Figure 2 shows the cross-section SEM image of the silicon film and the grain-filters. It can be seen that the grain-filters are filled by the liquid silicon completely. Next the film was pre-annealed in a furnace at 650oC for 2 hours to dehydrogenate the a-Si film. After the annealing, hydrogen concentration of a-Si film measured with TOF-SIMS was decreased from 6.7x1021cm-3 to 2-5x1019cm-3 (see Table 1), and film density, measured by XRR, increases from 1.96g/cm3 to 2.328g/cm3, of which the latter is exactly the same as that of the crystalline Si substrate. Then the crystallization of a-Si film was investigated using XeCl excimer laser (308nm) with a pulse duration of 25ns or 250ns at a substrate temperature of 450oC or 20oC, with fluences varying from 450 to 1400 mJ/cm2. Finally the sample was crystallized with laser pulse duration of 25ns at a substrate temperature of 450oC, with fluences varying from 450 to 700 mJ/cm2.

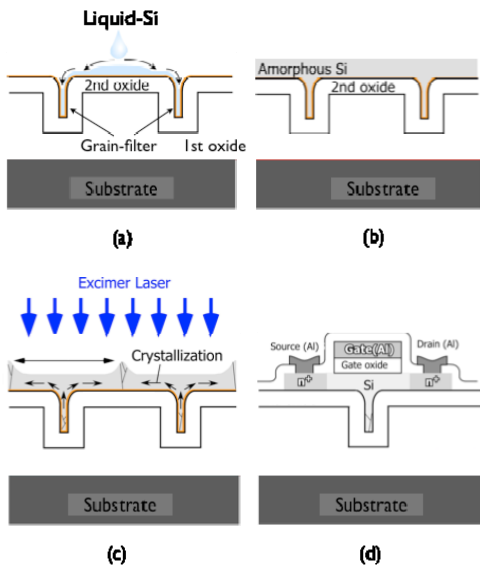

Figure 1. Schematic view of the fabrication process of the single-grain Si TFT using the liquid-Si

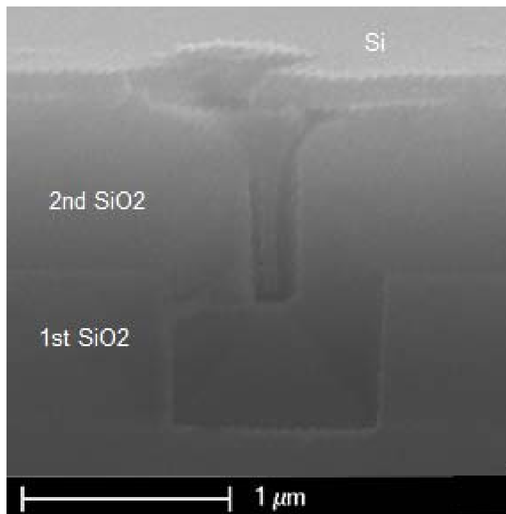

Figure 2. Cross-sectional SEM image of a-Si film

Table 1. Hydrogen content in the a-Si film, measured by TOF-SIMS

Sample	[H] (cm^{-3})
a-Si with spin-coated liquid Si	6.7e21
a-Si with spin-coated liquid Si after pre-anneal	2–5e19
LPCVD a-Si film	4.1e19

After patterning the Si film into islands, 36nm thick oxide was formed on the Si as gate oxide, with ICP oxidation growth at 250oC for 14nm, followed by PECVD TEOS deposition at 350 oC with 22nm. After aluminum gate formation, source and drain region were doped with 1x1016 ions/cm2 boron at 20keV for PMOS and 1x1016ions/cm2 phosphorus implantation at 70keV for NMOS transistors. The dopants are activated using the XeCl excimer laser at a fluence of 300mJ/cm2 at room temperature. The temperature of all process steps is lower than 650oC. Figure 3 is the optical microscopic image of the fabricated SG TFTs. Channel width and length are 1um for both.

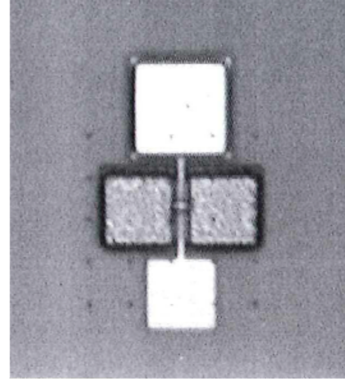

Figure 3. Optical microscopic image of fabricated SG-TFTs. The channel size is 1um by 1um

Results and discussion

Figure 4 shows the relationship of the crystalline grain size and the laser fluence under different conditions, which are short pulse (25ns) and 450oC, long pulse (250ns) and 450oC, short pulse and room temperature, and long pulse and room temperature. In general, the grain size increased with the energy density. After obtaining the largest grain, we observed ablation at the center of the grain filters. If we continued to increase the energy density, the ablation area will extend from the center of the grain filter to the whole grain filter region, and if the fluence was further increased, the a-silicon film would be ablated. Figure 4 also illustrates that if the same pulse duration is used, lower energy density was needed to get same grain size when the substrate temperature was higher, so the curve shifted left with lower substrate temperature. The maximum grain size does not change a lot with higher or lower substrate temperature. However, much larger grains were obtained when longer pulse was used, because ablation was observed at a higher energy density. The maximum grain size which could be obtained with long laser pulse was 3-4um, and with the short pulse was 1.6um.

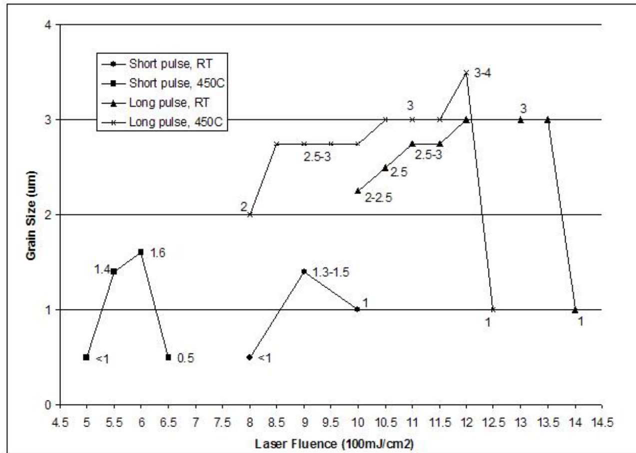

Figure 4, Chart of crystallization grain size vs. laser fluence

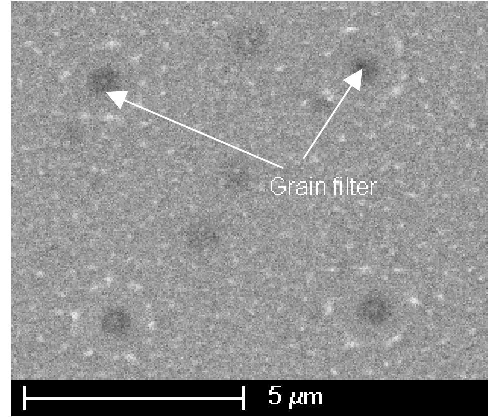

Figure 6. SEM image of Si film after crystallization. Pitch between the grain filters is 6 microns.

When processing the TFTs, the sample was crystallized with short pulse, at a substrate temperature of 450oC, and we have obtained Si grains with a maximum size of 1.6um with an energy density of 700mJ/cm2. Figure 5 and 6 show SEM image of surface of the Si film on a grain-filter array, before and after the laser crystallization, respectively. Si grains were successfully grown on top of the predetermined positions of the grain-filters. Figure 7 is a top-view SEM image of the silicon film, which shows that when we increased the energy density after getting the largest grain, ablation started from the center of the grain filters.

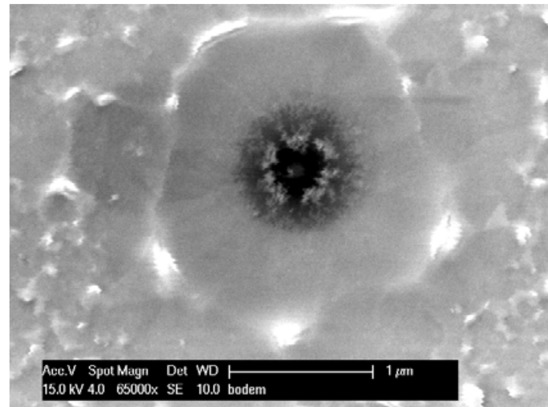

Figure 7, SEM image of center-ablated grain filter

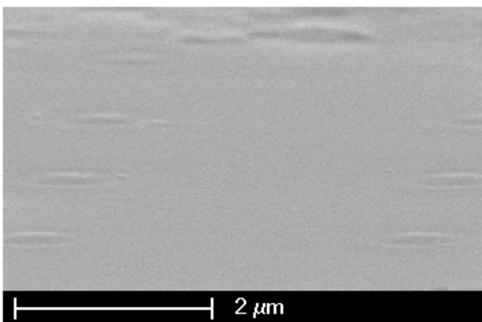

Figure 5. SEM image of a-Si film surface before crystallization

Figure 8 and 9 show the transfer characteristics of NMOS and PMOS SG-TFTs on the location-controlled Si grain. The carrier mobilities, which were estimated in the linear region at a low drain voltage, are 391 cm2/Vs for the electrons and 111 cm2/Vs for the holes. The carrier mobility is much higher than that of the poly-Si TFTs [1] because the channel is completely inside one single grain hence no grain boundary inside the active region. Figure 10 and 11 show the output characteristics of NMOS and PMOS transistors. While PMOS shows readily increase of Id from the origin, NMOS shows non-linear behavior. The high parasitic resistance may be caused by high resistance in the S/D region due to small thickness of the silicon layer. Table 2 is the summary of characteristic values for NMOS and PMOS SG-TFTs. Figure 12 shows the mobilities of the holes and electrons as a function of the laser fluences. For electrons the mobility decreases with the fluence while the mobility for holes reached the maximum with the laser fluence of 600mJ/cm2.

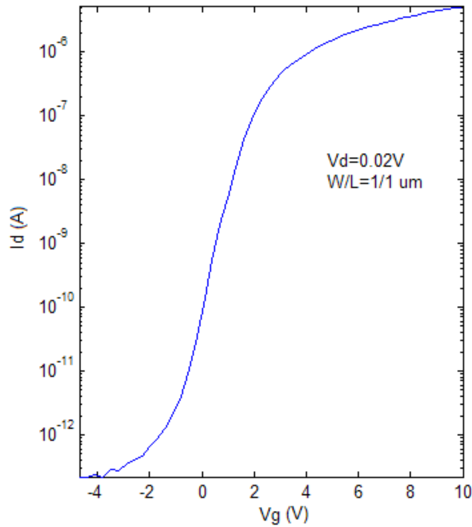

Figure 8. Transfer characteristic for NMOS SG-TFTs

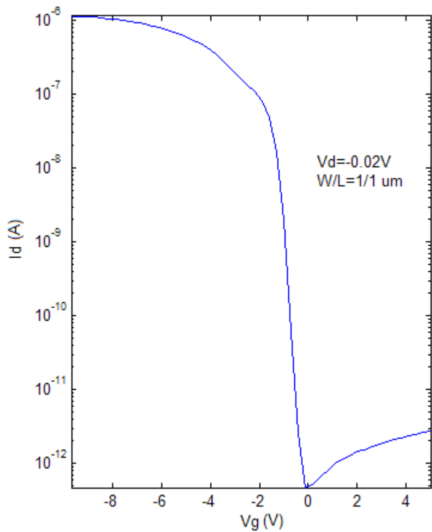

Figure 9. Transfer characteristic for PMOS SG-TFTs

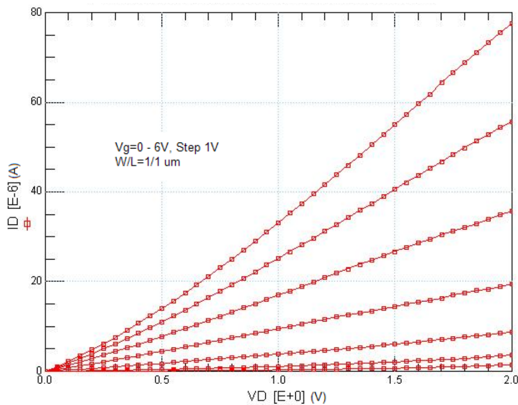

Figure 10. Output characteristics for NMOS SG-TFTs

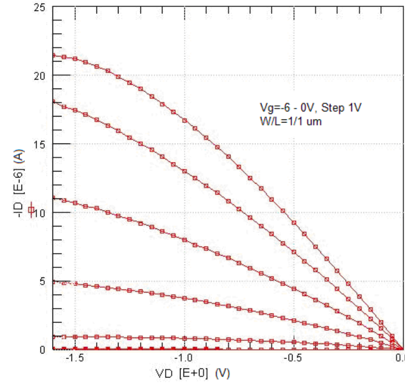

Figure 11. Output characteristics for PMOS SG-TFTs

Table 2. Summary of characteristic values for NMOS and PMOS SG-TFTs

TFT	NMOS	PMOS
μ_{FE} (cm^2/Vs)	391	111
V_{th} (V)	2.6	1.57
S (V/dec)	0.5	0.2
I_{on} (μA)	0.57	0.3
I_{leak} (pA)	0.59	0.46

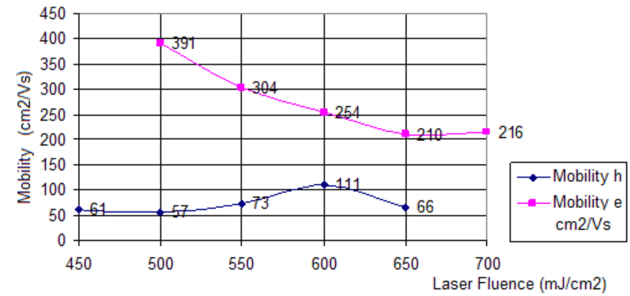

Figure 12. Electron and hole mobilities vs. laser energy density

Conclusion

We have fabricated single-grain Si TFTs on location-controlled Si grains with laser crystallization of spin-coated liquid Si film. The maximum grain diameter is 2um, and the mobilities for electrons and holes are 391 cm2/Vs and 111 cm2/Vs, respectively.

References:

[1] T. Shimoda, et al., Nature, 440 (2006) 783
[2] R. Ishihara, et al., Thin Solid Film, vol. 427 (2003) 77-85