

2nd JST International Symposium on Dependable VLSI Systems (DVLSI 2013)

December 6-7, 2013

Kikai Shinko Kaikan Building, Tokyo, Japan

Sponsored by JST CREST/DVLSI

Co-Sponsored by Kyushu Institute of Technology

In cooperation with

the IEEE Solid-State Circuits Society Japan Chapter (tentative)

the IEEE Solid-State Circuits Society Kansai Chapter (tentative)

the IEICE Electronics Society Technical Committee on Integrated Circuits and Devices (tentative)

the IEICE Information and Systems Society Technical Committee on Dependable Computing

This is an announcement of the second JST International Symposium of Dependable VLSI Systems to be held in Tokyo on December 6-7, 2013. The purpose of this meeting is to review and discuss the progress and outcome of a research program entitled, "Dependable VLSI Systems (DVLSI)" among professionals having special interest in the dependability of electronic systems. This unique program, sponsored by JST (Japan Science and Technology Agency), was initiated in 2007 for the purpose of developing basic VLSI technologies to enhance the dependability of systems. The program addresses various important issues of dependability ranging from the chip level all the way up to the systems level. Systems addressed include automotive, robotic, plant control, transportation, telecom, data processing to aerospace. The program consists of eleven (11) projects which has dealt with key issues, some arising from small feature sizes and others from design complexity. At the symposium this year, all eleven projects are reviewed including those which completed the term of five years and a half in March 2013. We will solicit guest speakers and panelists from various organizations of excellence where related objectives are being pursued. Invitation is being extended to everybody who has ever attended the past DVLSI meetings or to anybody who has special interest in the systems dependability and its implications in VLSI.

Venue

Kikai Shinko Kaikan Building,
3-5-8 Shibakoen, Minato-ku, Tokyo 105-0011 Japan

Access

1. 6-minute walk from Kamiyacho Sta., Tokyo Metro Hibiya Line
2. 8-minute walk from Onarimon Sta., Toei Mita Line
3. 10-minute walk from Akabanebashi Sta., Toei Oedo Line

<http://www.jspmi.or.jp/kaigishitsu/access.html>



Registration

Invited attendees: Invitation will be extended to solicit attendance.

General registration: welcome to pre-register at <http://www.dvlsi.jst.go.jp/english/index.html>

Registration Fee: free for all sessions, and 6000 JPY for banquet

Contact: symposium secretariat (k2tsujim@jst.go.jp or dvlsi@dvlsi.jst.go.jp)

Program Committees

Chair:	Seiji Kajihara	(Kyushu Institute of Technology)
Secretary:	Satoshi Ohtake	(Oita University)
Members:	Masahiko Yoshimoto	(Kobe University)
	Tomohiro Yoneda	(The National Institute of Informatics)
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Atsushi Hasegawa	(President, Renesas System Design Co., Ltd.)
Yoshio Masubuchi	(Senior Fellow, Toshiba Corp. Semiconductor & Storage Company)
Kazuo Yano	(Senior Chief Researcher, Hitachi Ltd. Central Research Lab.)
Koichiro Takayama	(Senior Director, Fujitsu Ltd.)

Principal Investigators and Research Themes

1. Hidetoshi Onodera (Kyoto University) URL <http://www.tamaru.kuee.kyoto-u.ac.jp/>
“Dependable VLSI platform using robust fabrics”
2. Shuichi Sakai (The University of Tokyo) URL <http://www.mtl.t.u-tokyo.ac.jp/index-e.html>
“Ultra Dependable VLSI by collaboration of formal verifications and architectural technologies”
3. Kazuo Tsubouchi (Tohoku University) URL <http://www.riec.tohoku.ac.jp/lab/it-21-mob/index-e.html>
“Development of Dependable Wireless System and Device”
4. Hiroto Yasuura (Kyushu University) URL <http://soc.ait.kyushu-u.ac.jp/SOC/>
“Modeling, Detection, Correction and Recovery Techniques for Unified Dependable Design”
5. Seiji Kajihara (The Kyushu Institute of Technology) URL <http://aries3a.cse.kyutech.ac.jp/>
“Circuit and system mechanisms for high field reliability”
6. Masahiko Yoshimoto (Kobe University) URL <http://www28.cs.kobe-u.ac.jp/en/>
“Dependable SRAM Techniques for Highly Reliable VLSI System”
7. Tomohiro Yoneda (National Institute of Informatics) URL http://www.nii.ac.jp/staff/Yoneda_Tomohiro.shtml
“Development of Dependable Network-on-Chip Platform”
8. Mitsumasa Koyanagi (Tohoku University) URL <http://www.sd.mech.tohoku.ac.jp/Site/Home.html>
“Three-Dimensional VLSI System with Self-Restoration Function”
9. Ken Takeuchi (Chuo University) URL http://www.takeuchi-lab.org/index_e.htm
“Dependable Wireless Solid-State Drive (SSD)”
10. Takeshi Fujino (Ritsumeikan University) URL <http://www.ritsumeik.ac.jp/se/re/fujinolab/index-e.html>
“The Design and Evaluation Methodology of Dependable VLSI for Tamper Resistance”
11. Nobuyuki Yamasaki (Keio University) URL <http://www.ny.ics.keio.ac.jp/>
“Fundamental Technology on Dependable SoC and SiP for Embedded Real-Time Systems”

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December 6, 2013

13:00 Opening Remarks from Shojiro Asai (Chair: S. Kajihara)

13:20 Keynote: Challenges at Circuits Designs for Nonvolatile Memory and Logics
in Dependable Systems

Meng-Fan (Marvin) Chang, National Tsing Hua University

14:00 Break

14:20 Session 1: Wireless Communication and 3D Connectivity (Chair: H. Ishikuro)

Invited Talk: Heterogeneous Networks for Dependable Wireless Access
and the 1000x Capacity Challenge

Valentin Gheorghiu, Qualcomm Standards and Industry Organizations

CREST DVLSI presentations:

1. Development of Dependable Wireless System and Device

K. Tsubouchi

2. Dependable Wireless Solid-State Drive (SSD)

K. Takeuchi

3. Three-Dimensional VLSI Systems with Self-Restoration Function

M. Koyanagi

16:00 Break

16:20 Session 2: System Testing and Error Tolerance (Chair: M. Inoue)

Invited Talk: Dynamic Adaptation for Resilient Integrated Circuits and Systems

Krishnendu Chakrabarty, Duke University

CREST DVLSI presentations:

1. Dependable SRAM Techniques for Highly Reliable VLSI Systems

M. Yoshimoto

2. DART: Dependable Architecture with Reliability Testing

- Failure Prediction for High Field Reliability -

S. Kajihara

17:40 Break

18:00 Banquet (-19:30)

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December 7, 2013

- 9:00 Session 3: Soft Error Resilience and Variability-Aware Design (Chair: H. Ochi)
Invited Talk: Cross-layer Approaches for Resilient System Design
Mehdi B. Tahoori, Karlsruhe Institute of Technology
CREST DVLSI presentation:
1. Soft-error and Variability Resilience in Dependable VLSI Platform
H. Onodera
2. SRAM Soft Error Rate Estimation Tool with Nuclear Reaction Simulator
H. Kawaguchi
- 10:20 Break
- 10:40 Session 4: Real Time Processing under Various Environmental Condition (Chair: M. Imai)
Invited Talk: Deterministic Ethernet as Reliable Communication Infrastructure for
Distributed Dependable VLSI Systems
Wilfried Steiner, TTTech Computertechnik AG
CREST DVLSI presentations:
1. Development of Dependable Network-on-Chip Platform
T. Yoneda
2. Fundamental Technology on Dependable SoC and SiP for Embedded Real-time
Systems
N. Yamasaki
- 12:00 Lunch
- 13:00 Poster Session
- 14:00 Session 5: Trusted Computing and Formal Verification of Designs (Chair: M. Yoshikawa)
Invited Talk: Putting Trust in Automotive Electronics
Camille Vuillaume, ETAS K.K.
CREST DVLSI presentations:
1. The Design and Evaluation Methodology of Dependable VLSI for Tamper Resistance
T. Fujino
2. FOF (Functionally Observable Fault): A unified mode for testing and debugging
- ATPG and application to debugging -
Masahiro Fujita, University of Tokyo
- 15:20 Break
- 15:40 Panel Discussion: What is expectation and difficulty to realize dependable systems?
(Moderators: M. B. Tahoori and N. Yamasaki)
Invited Talk: "Real Systems Are Usually Not Perfect, So Why Design Assuming They Are"
Roger Barth, Micron Technology
Panelists: R. Barth, W. Steiner and C. Vuillaume
- 17:00 Closing Remarks