Dependable Wireless Solid-State Drive (SSD)

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Objectives of Research

- Wireless SSD/Memory card and its host system
- Robust against memory cell error, contact error, ESD, EMI and waterproof
- High-speed near field wireless communication
  - Target: 10-50Gbps at 1mm distance
- Wireless power delivery with MHz load variability
  - Target: 1-3W
11 ISSCC Presentations

- **ISSCC 2014**
  - Takeuchi “Hybrid Storage of ReRAM/TLC Flash for Cloud Data Centers”
  - Kuroda, Ishikuro “Electromagnetic Clip Connector for In-vehicle LAN”

- **ISSCC 2013**
  - Takeuchi “Unified Solid-State Storage”
  - Kuroda, Ishikuro “A 0.15-mm-Thick Non-Contact Connector for MIPI”
  - Kuroda “Inductive-Coupling Wake-Up Transceiver for Non-Contact Memory Card”
  - Kuroda “Retrodirective Transponder Array with Universal On-Sheet Reference for Wireless Mobile Sensor Networks”

- **ISSCC 2012**
  - Takeuchi “Error-Prediction LDPC”
  - Kuroda, Ishikuro “7Gb/s/Link Non-Contact Memory Module”
  - Ishikuro “Voltage-Boosting Wireless Power Delivery System”

- **ISSCC 2011**
  - Takeuchi “Asymmetric Coding for SSD”
  - Kuroda, Ishikuro “12Gb/s non-contact interface”
 Dependable Memory System

- Data retention error and program disturb error become worse as the memory cell is scaled.
- ECC should be improved with the device scaling.

![Graphs showing data retention error and program disturb error](image)

- LDPC ECC is needed.
- Acceptable BER of ECC:
  - 1KByte codeword (BCH)
  - 512Byte codeword (BCH)

Feature size (nm) vs. Acceptable BER of ECC

Programmed cell

Disturbed cells
Highly Dependable Memory System

- In total, >1000X reliability improvement

<table>
<thead>
<tr>
<th>Year</th>
<th>Description</th>
<th>Reliability Improvement</th>
</tr>
</thead>
<tbody>
<tr>
<td>2009</td>
<td>Adaptively change ECC correctability (IMW2010:Dynamic Codeword Transition ECC)</td>
<td>17X</td>
</tr>
<tr>
<td>2010</td>
<td>Correct the asymmetric memory error (ISSCC2011:Asymmetric Coding)</td>
<td>20X</td>
</tr>
<tr>
<td>2011</td>
<td>Fast and Extremely Reliable LDPC (ISSCC2012:Error Predicting LDPC)</td>
<td>11X</td>
</tr>
<tr>
<td>2012</td>
<td>Unified Storage System (ISSCC2013:Riverse Mirroring)</td>
<td>32X</td>
</tr>
<tr>
<td>2013</td>
<td>Integrated Error Correction of ReRAM and Flash Memory (ISSCC 2014)</td>
<td>22X</td>
</tr>
</tbody>
</table>
Asymmetric Coding (ISSCC 2011)

- Increase “0” for Upper page and “1” for Lower page
- X20 Better Reliability

Data retention error: Vth decrease due to the charge leakage

# of cells

0 → 1 error (Lower page)
1 → 0 error (Upper page)

Asymmetric Coding

Overhead

Modified data1: 0 0 1 0
Bit flip

Modified data2: 1 1 0 1
Do NOT flip

Data unit1

Data unit2

Flag

e.g. Code length: 4

NAND Flash memories

SSD controller

Daughter board
Error Predicting LDPC (ISSCC 2012)

- Compensate the capacitive interference by using the neighboring cell data

- Compensate the Vth decrease during data retention by write/erase cycles and data retention time data

- X11 Better Reliability

Conventional $V_{ref1}$ $V_{ref21}$ Vth decrease during data retention

Proposed $V_{ref}$ $V_{ref}$ $V_{ref}$

FG-FG interference

# of cells

1 1 0 1 0 0 1 0
Unified Solid-State Storage (ISSCC 2013)

- Unified Storage Controller integrating SSD controller and RAID controller.
- Use ReRAM as NV-Cache.
- X32 Better Reliability

![Diagram of Unified Solid-State Storage System]

Key Features:
1. Reverse-mirroring (RM)
2. Error-reduction synthesis (ERS)
3. Page-RAID
4. Error-masking (EM)
Reverse-mirroring (ISSCC 2013)

Assign data to primary and mirror Storage to minimize errors.

Program data

Mirroring buffer (ReRAM)

Page position inversion

Write from Page₀

Primary NAND

D.R. BER

Page #

Source-line side

Bit-line side

Program disturb BER

W/E cycle: 10k

Page number

Data retention BER

W/E cycle: 10k

Page number

10 hours @ 85 °C

Error increment trend

2Xnm

Program data

Page #

Pair

Pair

Pair

Pair

Write from Page₀

Mirrored NAND

Extension board for storage (NAND flash)

Storage controller board

Extension board for storage (NVMs)

Storage controller chip
### Page RAID (ISSCC 2013)

<table>
<thead>
<tr>
<th>Storage</th>
<th>HDD</th>
<th>NAND (USSS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Failure</td>
<td>Disk (Mechanical)</td>
<td>Page (Bit-errors)</td>
</tr>
</tbody>
</table>

#### Redundancy Scheme

<table>
<thead>
<tr>
<th>RAID</th>
<th>Page-RAID</th>
</tr>
</thead>
<tbody>
<tr>
<td>- HDD1</td>
<td>• No disk exchange</td>
</tr>
<tr>
<td>- HDD2</td>
<td>• Low cost</td>
</tr>
<tr>
<td>- HDD3</td>
<td>Replace</td>
</tr>
</tbody>
</table>

- No disk exchange
- Low cost
Page RAID (ISSCC 2013)

- RAID optimized for flash memory, Repair failed word-line
- Store parity in ReRAM
- >X10 Better Reliability

- ReRAM is suitable for parity buffer due to large endurance cycle.
Non-contact Connector

Conventional Connector
Mechanical contacts

Issues and challenges
- dependability (non-waterproof)
- signal integrity (crosstalk, reflection)
- farm factor (big, thick, heavy)
- assembly (manual labor, large force)

Non-contact Connector
Near-field coupling

+ non-contact
+ no mechanical structure
+ impedance controlled
+ easy to put on and take off
Transmission Line Coupler (TLC)

Length ($L$)

Port 1

Port 2

Width ($W$)

Coupling Gain [dB]

Frequency [GHz]

-40 -30 -20 -10 0

0 5 10 15 20 25 30

$L=3$mm

$L=5$mm

$L=7$mm

Misalignment ($h$) [mm]

W=0.4mm

0 0.2 0.4 0.6

-40 -30 -20 -10 0
Applications

**Memory Card**
- High speed: 50x (12Gb/s)
- Low power: 1/500
- Sealing: waterproof

ISSCC2011, ISSCC2013

**Display**
- Thin: 1/10 (0.15mm)
- High speed: 10x (6Gb/s)
- Low energy: 1/10 (16pJ/b)

ISSCC2013

**Transmission Line Coupler (TLC)**

**DIMM**
- High speed: 5x (12.5Gb/s)
- Multi-drop bus

ISSCC2012, CICC2012

**In-vehicle LAN**
- Reduced weight: 30%
- EMC

ISSCC2014

**Mobile Terminal**
- Small size & Low cost

**Dependable Assembly**

**SD Memory Card**
- High speed: 50x (12Gb/s)
- Low power: 1/500
- Sealing: waterproof

ISSCC2011, ISSCC2013

**LCD Display**
- High speed: 10x (6Gb/s)
- Low energy: 1/10 (16pJ/b)

ISSCC2013

**Thin Display**
- High speed: 10x (6Gb/s)
- Low energy: 1/10 (16pJ/b)

ISSCC2013

**Mobile Terminal**
- Small size & Low cost

**Dependable Assembly**

**Transmission Line Coupler (TLC)**

**DIMM**
- High speed: 5x (12.5Gb/s)
- Multi-drop bus

ISSCC2012, CICC2012

**In-vehicle LAN**
- Reduced weight: 30%
- EMC

ISSCC2014

**Automotive, Computer**
- High speed & Low error
Memory Card (ISSCC2011)

Wireless Memory Card
NAND Flash Memory Chip
Nested Clover Coils for Simultaneous Power/Data Transmission

Host Chip

20mm x 20mm Power Link Coil
75mA_{rms} 13.56MHz

$2^{31}-1$ PRBS @ 12Gb/s

BER vs. Data rate [Gb/s]
BER vs. Delay Time [ps]

Power Link ON
Power Link OFF
Timing Margin = 0.5 UI
LCD Module (ISSCC2013)

- LCD Module
- TLC 0.15mm-Thick
- Host Board

Table:

<table>
<thead>
<tr>
<th>Port</th>
<th>Frequency [GHz]</th>
<th>Coupling Gain [dB]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 1</td>
<td>2</td>
<td>-10</td>
</tr>
<tr>
<td>Port 2</td>
<td>8</td>
<td>20dB</td>
</tr>
<tr>
<td>Port 3</td>
<td>2</td>
<td>-30</td>
</tr>
<tr>
<td>Port 4</td>
<td>10</td>
<td>-40</td>
</tr>
</tbody>
</table>

- 2 Ports in one TLC
- 2Gb/s x 2 Links = 4Gb/s/coupler
- 305 ps

Graph:

Coupling Gain [dB] vs. Frequency [GHz]

- S_{31}
- S_{41}

Confidential
Memory Bus (ISSCC2012, CICC2012)

Number of Modules vs Data Rate [Gb/s/lane]

- TLC: 12.5Gb/s 5Drops
- ISSCC’12, CICC’12
- DDR4
- ISSCC’11
- JSSC’12
- JSSC’13
- ISSCC’03

Controller #1 #2 #3 #4 #5

DRAM TLC

Confidential
“An Electromagnetic Clip Connector for In-vehicle LAN to Reduce Wire Harness Weight by 30%” (Paper 30.6)
Summary: Non-Contact Connector

**SD Memory Card**
- High speed: 50x (12Gb/s)
- Low power: 1/500
- Sealing: waterproof
- ISSCC2011, ISSCC2013

**LCD Display**
- Thin: 1/10 (0.15mm)
- High speed: 10x (6Gb/s)
- Low energy: 1/10 (16pJ/b)
- ISSCC2013

**Transmission Line Coupler (TLC)**

**DIMM**
- High speed: 5x (12.5Gb/s)
- Multi-drop bus
- ISSCC2012, CICC2012

**In-vehicle LAN**
- Reduced weight: 30%
- EMC
- ISSCC2014

**Mobile Terminal**
- Small size & Low cost

**Dependable Assembly**

**Automotive, Computer**
- High speed & Low error
Dependable Wireless Power Delivery System

Small size, battery-less application

Requirement:
Fast load tracking and low EMI

Switch between $f_{res}$, and $f_{res}/3$
Single-Channel Dual-Output WPD System

$f_{in}(6.78\text{MHz})$  

$T_X$

$C_1$

$C_2$

$C_3$

$V_{b}$$\rightarrow$

$V_{ref}$

$V_{OH}$

$V_{OL}$

△Σ Controller

Amp Buffer

Diode Driver

PRS-PWM Module

Duty Controller

Power Controller

ISSCC2012
A-SSCC2013

(21/24)
Test Chip and WPD Module

Coil size
2cm x 2cm

Resonance capacitor: 5
Smoothing capacitor: 2
Power Efficiency and Output Regulation

- Output voltage regulated at 16V and 8V
- Power efficiency: 40%
Fast Load Tracking and EMI Reduction

$P_{OH}$ 0.341W - 0.157W

$P_{OL}$ 0.085W - 0.206W

$V_{OH}(16V)$

$V_{OL}(8V)$

Mode control

Load transition point

Graph showing spurious emissions with and without ΔΣ modulation, indicating an 8dB improvement at a certain power setting.