

**JST International Symposium on
Dependable VLSI Systems 2012**

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“VLSI design and test for enhanced systems dependability”

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Program term: FY2007~2014

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- In its 6th year of the 8 year term

*CREST: <http://www.jst.go.jp/kisoken/crest/en/index.html>

Attributes, Threats, and Means in Dependability as defined by IFIP:



Attributes	way to assess the dependability of a system
Availability	readiness for correct service
Reliability	continuity of correct service
Safety	absence of catastrophic consequences on the users/environment
Integrity	absence of improper system alteration
Maintainability	ability for a process to undergo modifications and repairs
Threats	things that can affect the dependability of a system
Fault	defect in a system
Error	discrepancy between the intended and actual behavior of a system
Failure	system behavior that is contrary to its specification
Means	ways to increase a system's dependability
Prevention	preventing faults being incorporated into a system
Removal	fault removal during development and removal during use
Forecasting	prediction of faults to remove them or circumvent their effects
Tolerance	putting fault-tolerant mechanisms in place

Rationale for research in DVLSI

VLSI: Is the component key to systems of all kinds. Its dependability is at the foundation of systems dependability.

Problems: The dependability of VLSI is actually being increasingly more threatened.

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Threats arising from miniaturization

Variations in dimensions, shapes, doping densities,

Decrease in S/N ratio (radiation, EMI, fixed and floating charges),

Aggravating wear/fatigue phenomena (NBTI, hot carriers, electro-migration).

Threats arising from increased complexity

Enhanced functionality (id, encryption,---)

Multiple- Many-core architecture, multi-thread operation,

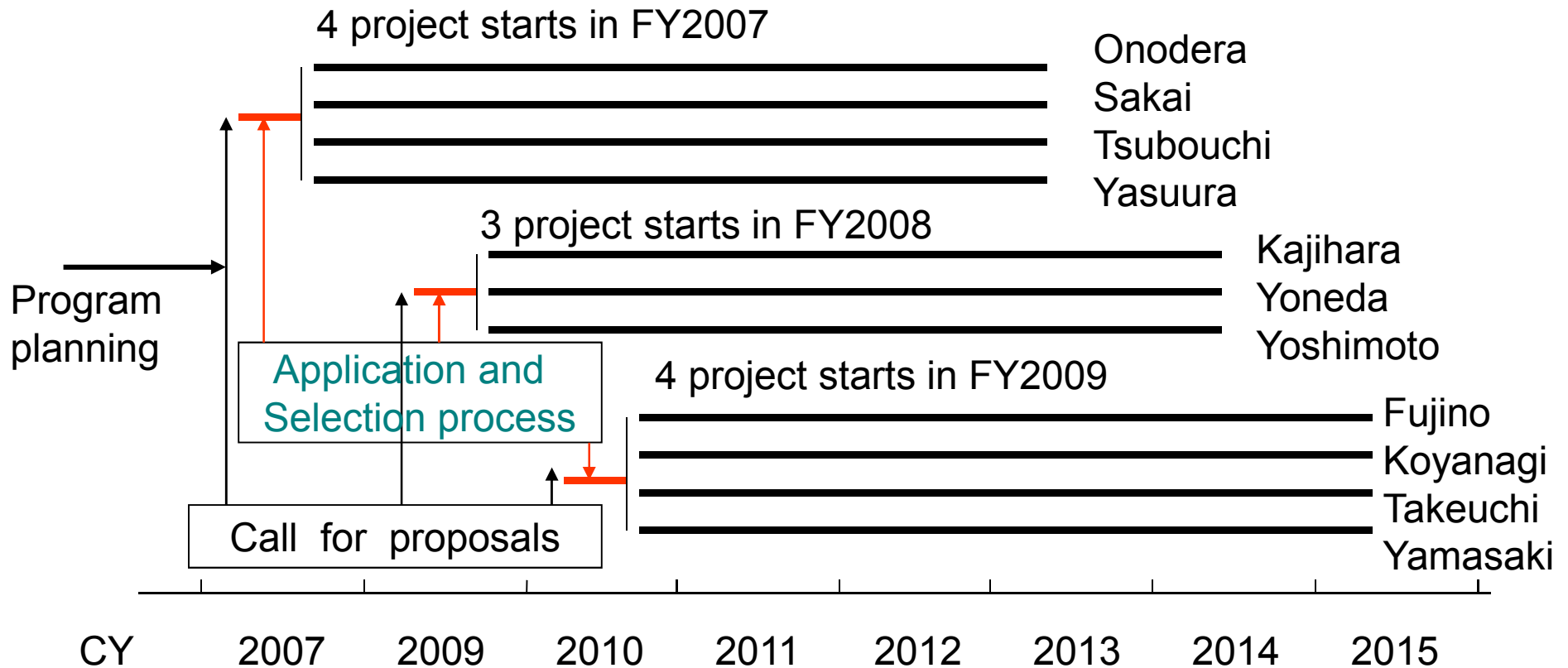
Heterogeneous integration

Analog, digital, nonvolatile, network, sensors, actuators, etc.

Mission of the DVLSI Program:

1. Contain Rising Threats within VLSI (Component Supposed to be Most Dependable) by Design and/or Testing
2. Provide New Functionalities in VLSI which Improve Dependability at the Systems Level

Selection and Terms of the DVLSI Projects



Program Term: 2007- 2015

DVLSI JST/CREST Program 'Dependable VLSI Systems'

Applications eyed and Approaches taken



Application	Space	Plant Control Transportation	Robot	Auto	Information Telecom	Finance Medical	Consumer
Onodera	Reconfigurable Processor, FF Design, Layout for Manufacturability						
Sakai	Failure-Resistant Architecture, Formal Design Verification						
Tsubouchi		Wide Bandwidth RF, FDE, Coding,, Connectivity, Heterogeneous Interface					
Yasuura	Systems-Level Soft-error Simulation, Soft-error-resistant Circuit/Systems Design						
Kajihara	Design/Test for Field Dependability						
Yoshimoto		Soft-Error-Resistant Memory, Systems-Level Simulation					
Yoneda		Networked Multi-Core Systems					
Koyanagi		Dependable 3D Processor for Image-Recognition					
Takeuchi		Wireless Solid-State Drive, Wireless Interconnect, Wireless Power					
Fujino				Tamper-Resistant Circuits, Tamper-resistance test			
Yamasaki	Real-time OS, controller, and packaging for Hard-Real-Time applications						

Areas DVLSI Projects cover:



Application

System

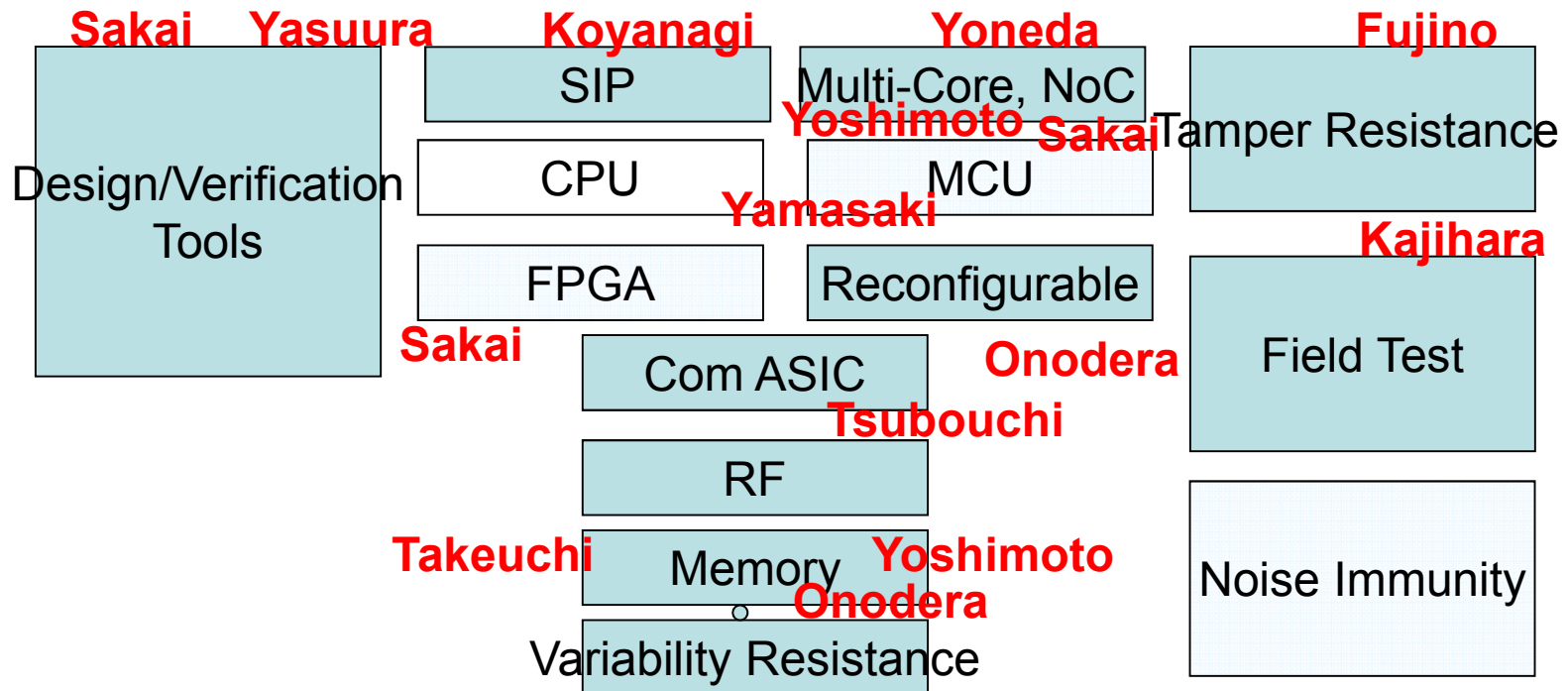
Reconfigurable

Operating System

Real-Time OS

Yamasaki

LSI System



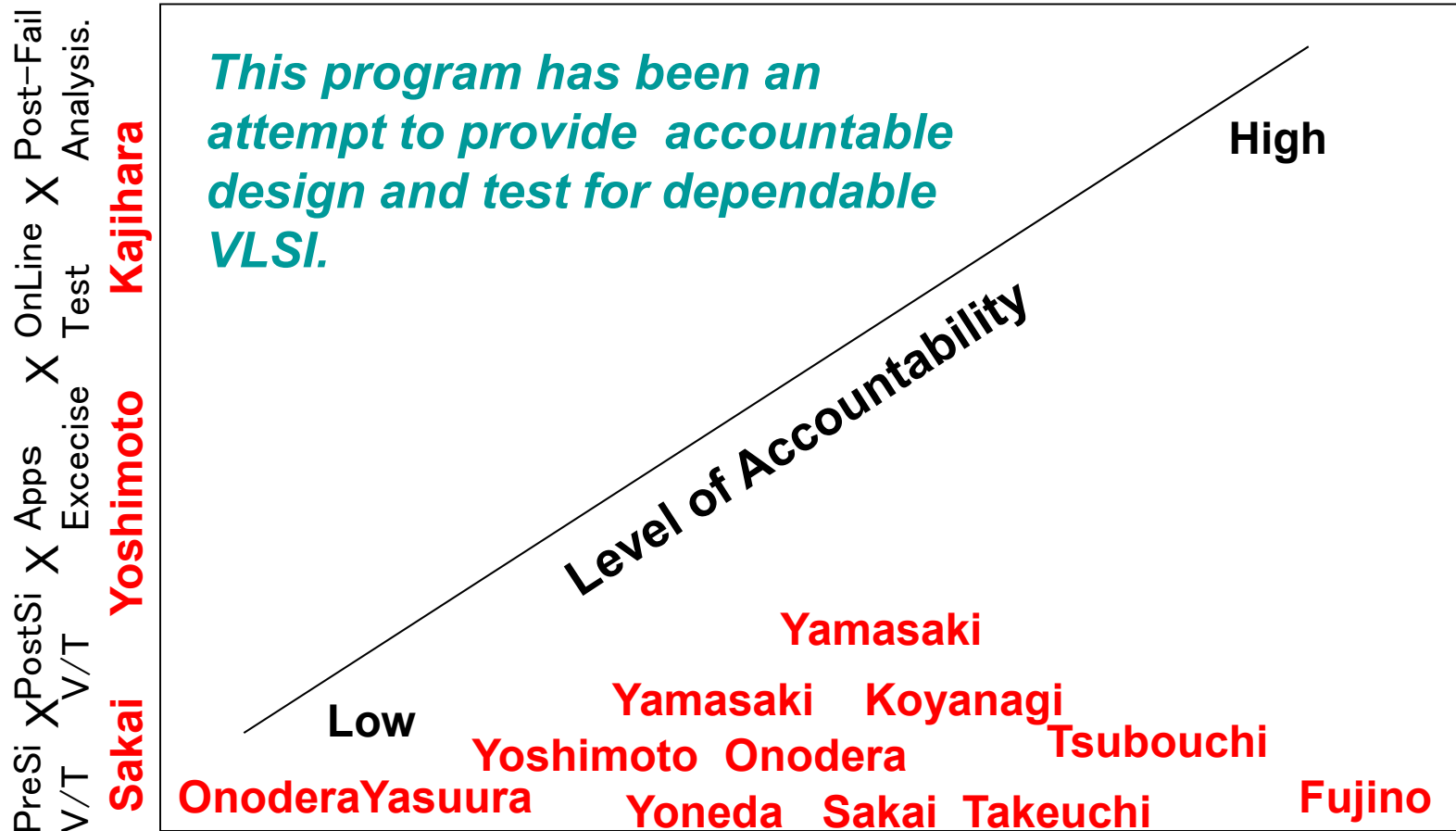
D/V tools

Chip Concept, IP Core

Test tools

VLSI Dependability = Π (Strength of Means against Threat) x Π (Coverage of Verification and Test)

Π Exhaustiveness of Verification, Test



variability soft-error noise redundant connectivity tamper
 resistance resistance immunity circuits resistance

Π Strength of **Means** against Threat (Robustness of Technology)





Thanks to the Organizing Committee Members:

Chair: Hidetoshi Onodera (Kyoto University)

Secretary: Masanori Hashimoto (Osaka University)

Members: Mitsumasa Koyanagi (Tohoku University)

Masahiro Goshima (University of Tokyo)

Suguru Kameda (Tohoku University)

Hiroshi Oguma (Toyama National College of Technology)

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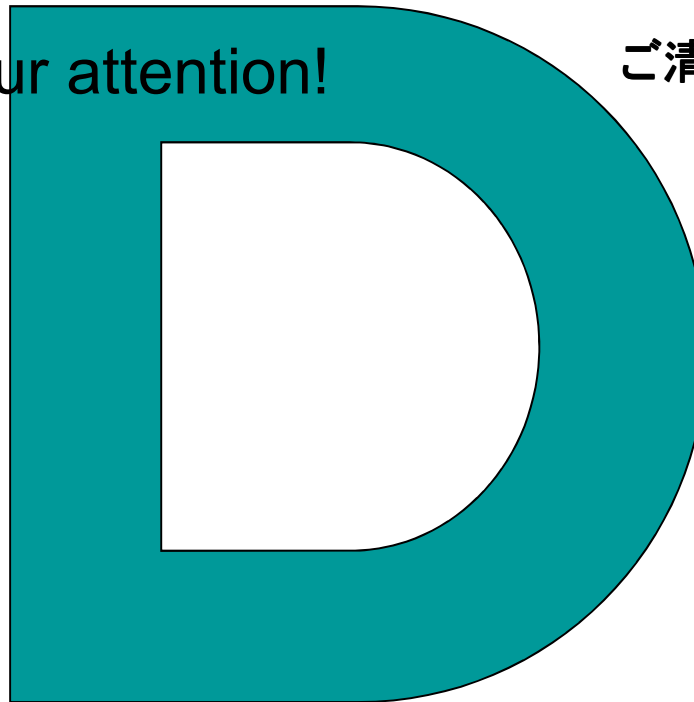


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Thank you for your attention!

ご清聴ありがとうございました



For more details, please visit the URL:

<http://www.dvlsi.jst.go.jp/>

<http://www.dvlsi.jst.go.jp/english/index.html>