Modeling, Detection, Correction and Recovery Techniques for Unified Dependable Design

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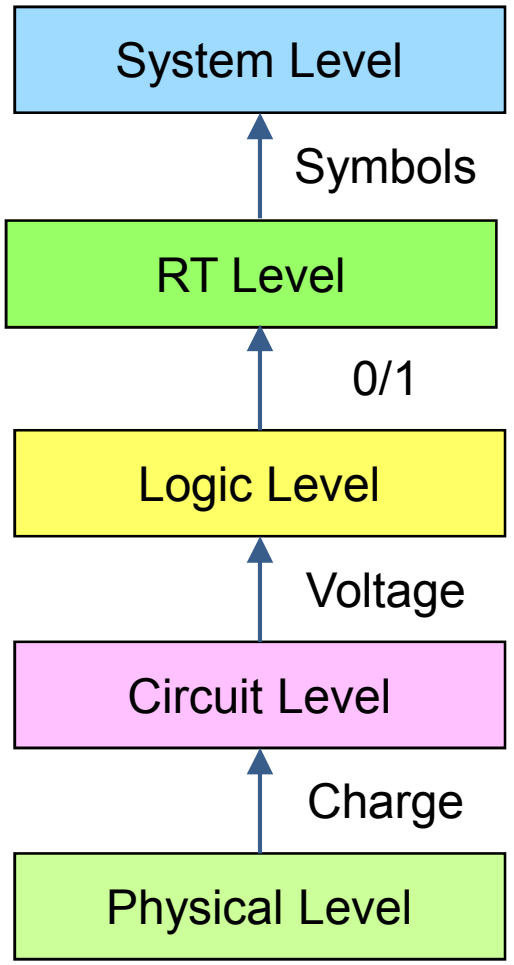
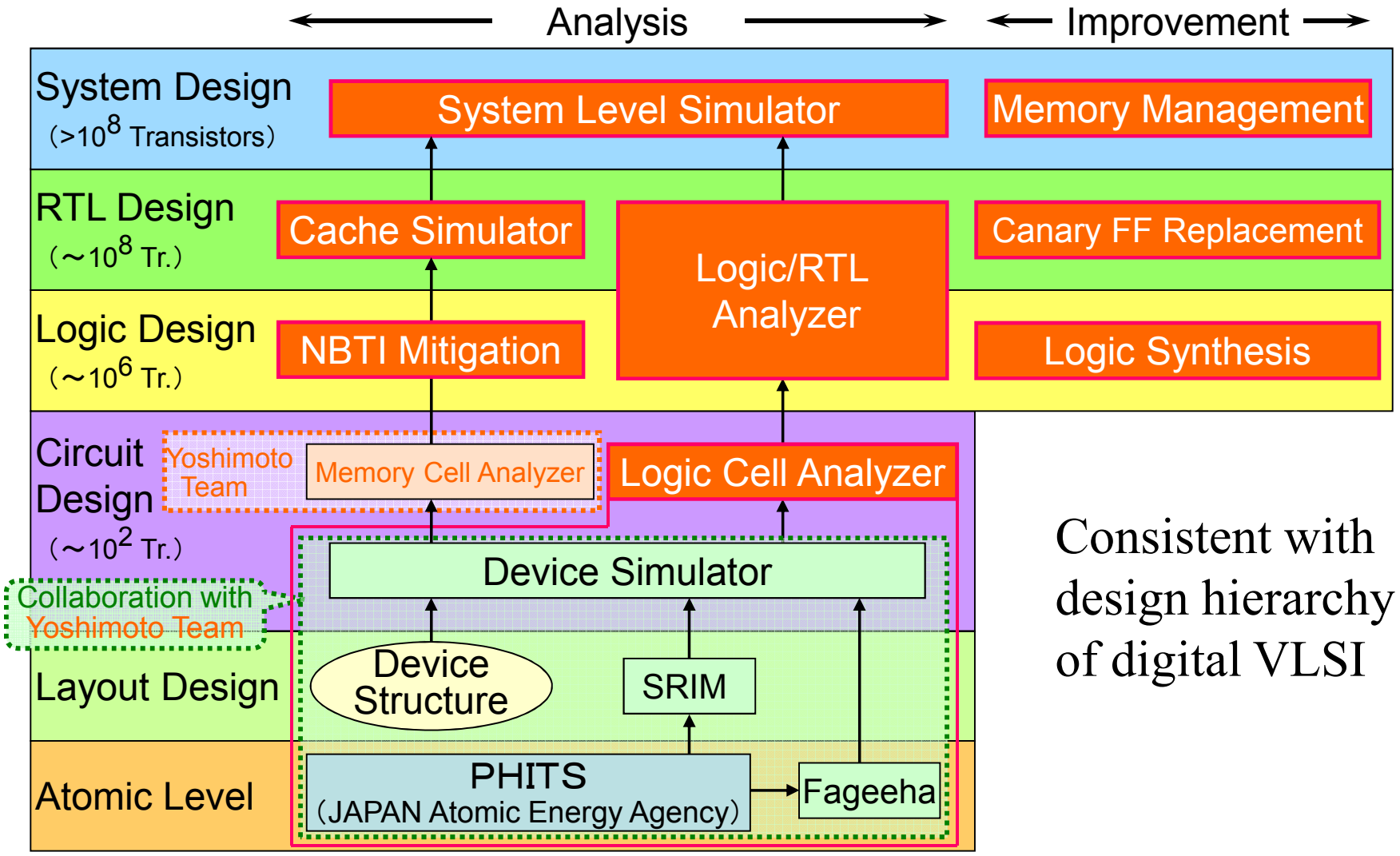
Analysis of Dependability in VLSI Design

- Analysis techniques of dependability for hierarchical VLSI system design are required.
- Error in the lower level should be modeled in different signals in the upper level.
- In most conventional researches, error models are supposed independently and dependability is analyzed in each level.
- We developed a tool chain, which can analyze dependability from the results in the lower level for soft error of digital VLSI.
  - Techniques for transfer error model from analyzed results in the lower level
  - Reduction algorithms of the computation time of analysis against the rapid increase of the number of transistors in the upper levels
- We also developed other technologies for dependable VLSI design
  - Resilient design by Canary FFs
  - Trade-off between design for testability and security

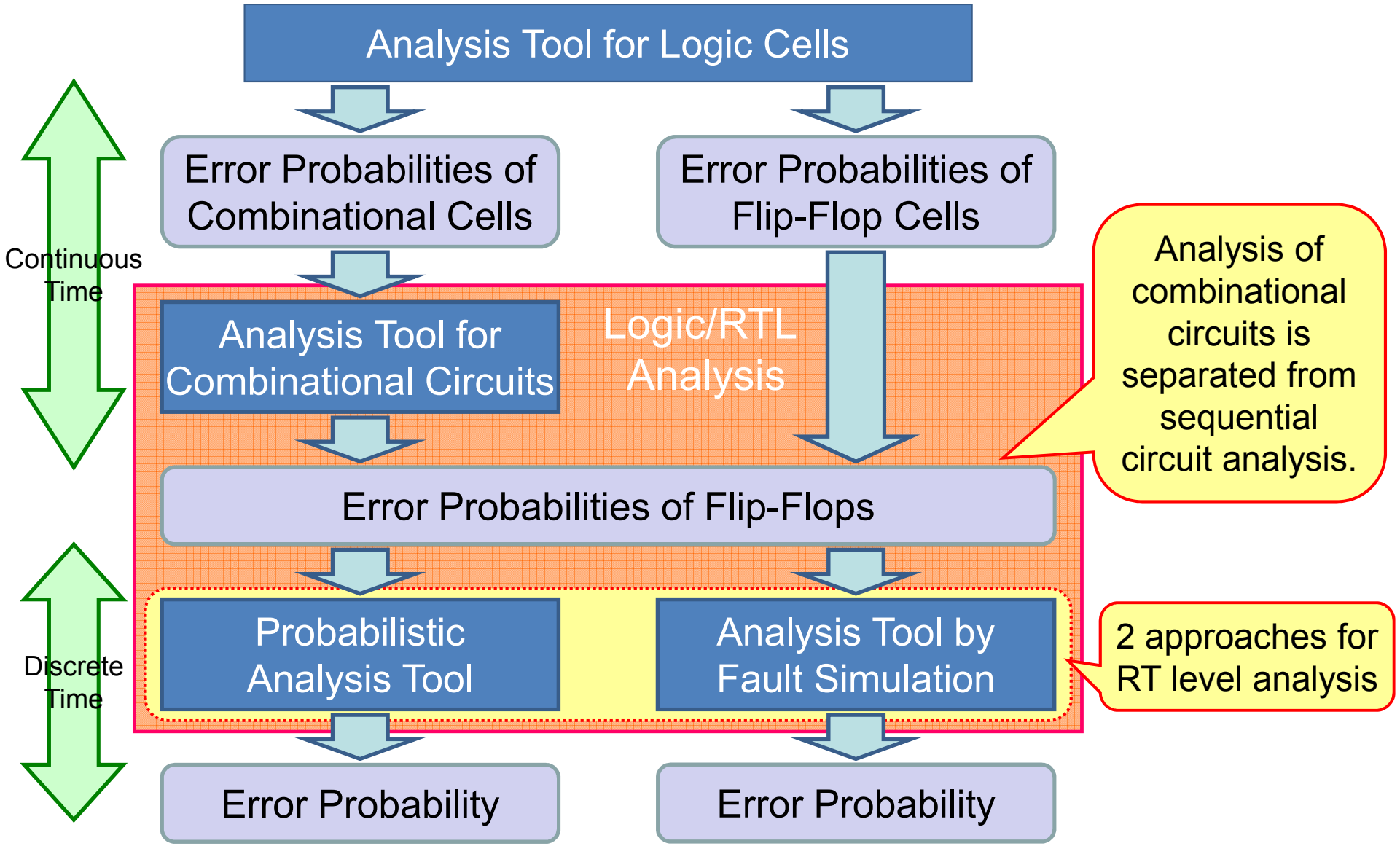


Tool Chain for Soft Error Tolerance

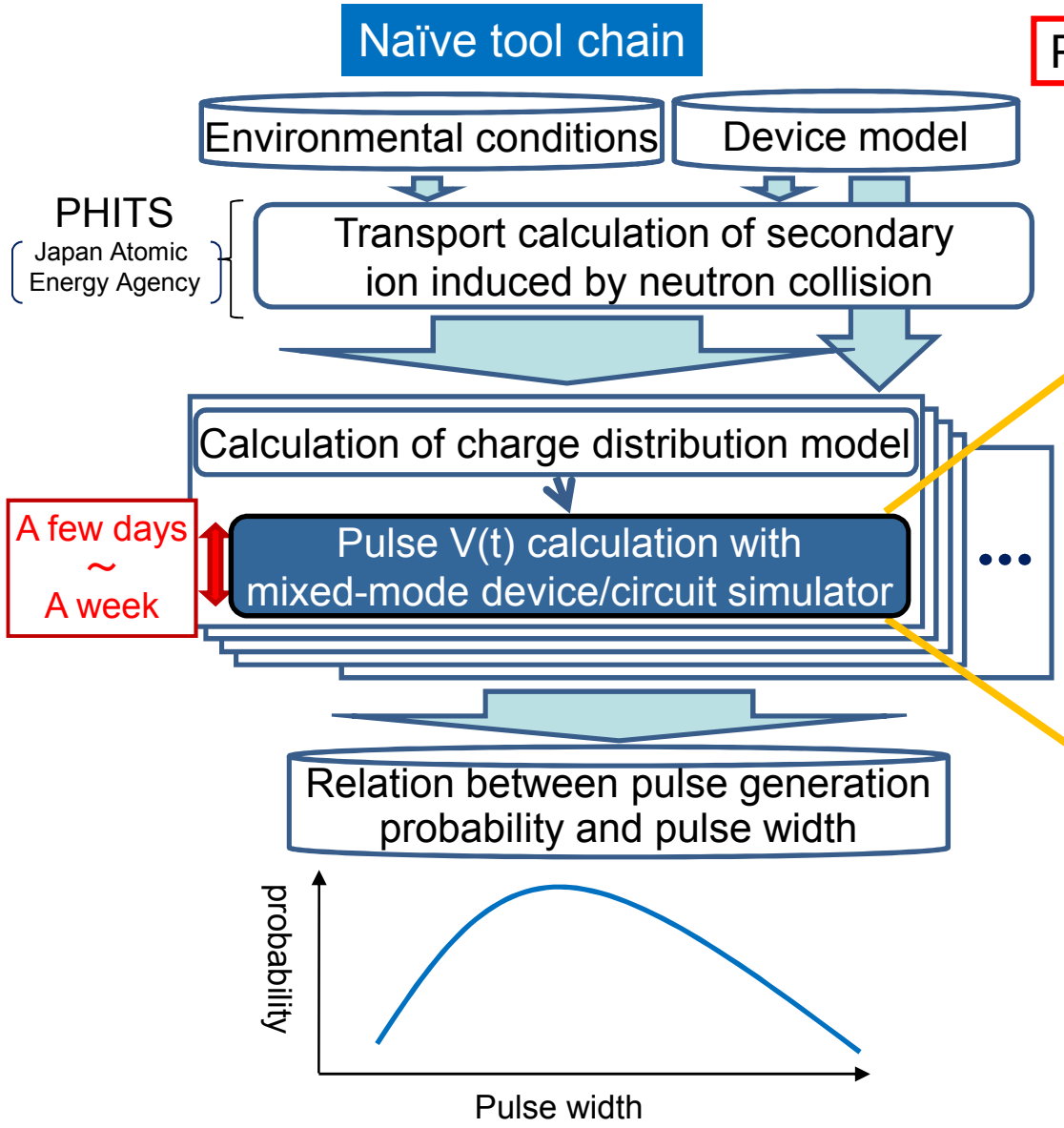


Consistent with design hierarchy of digital VLSI

Error Models and Analysis Tools



Analysis Tool for Logic Cells



Problem

Device simulation must be iterated for a lot of times to achieve highly accurate estimation
⇒impractically long run-time

Proposed Method

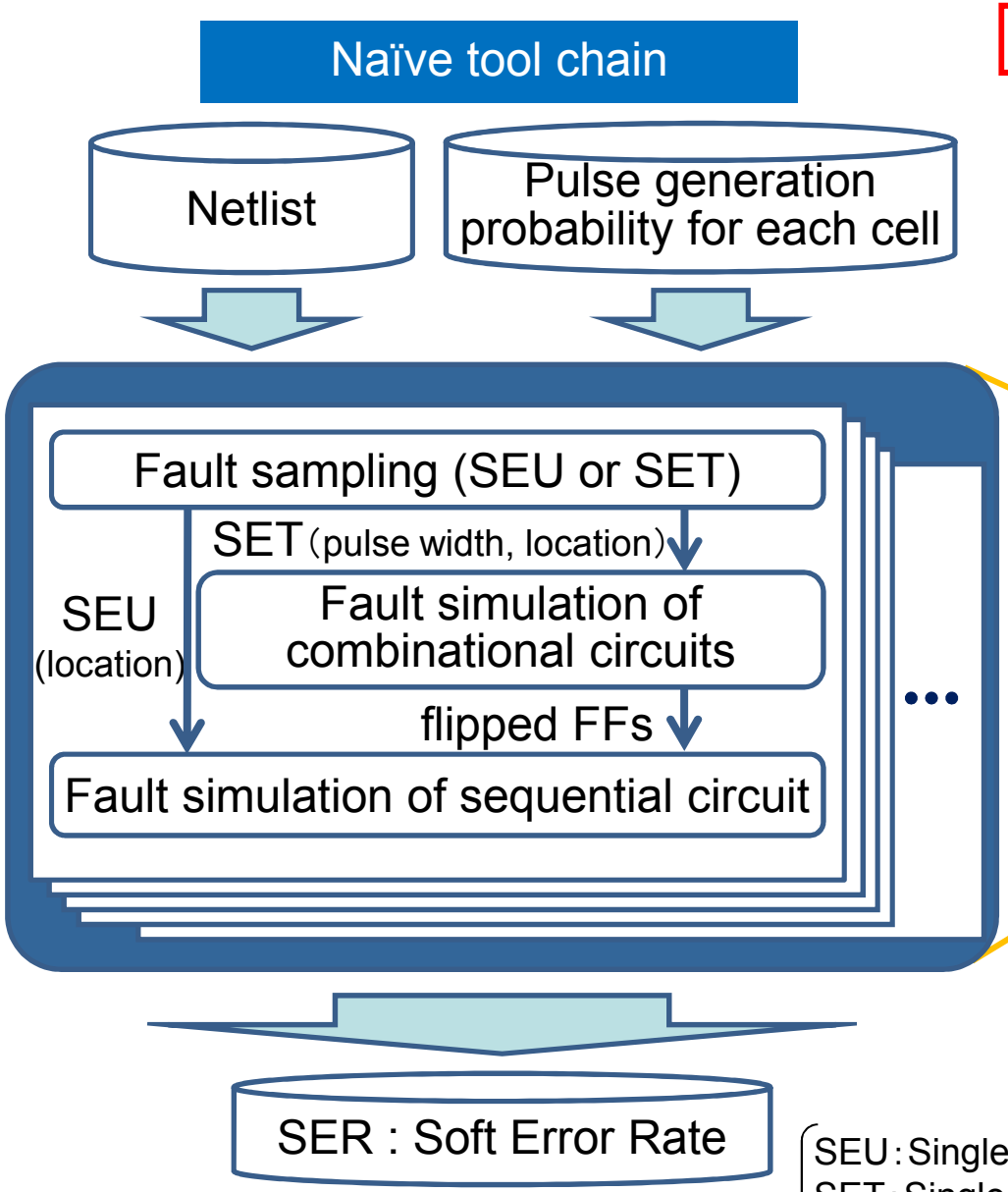
Approximation of noise electric current model using the amount of collected charge

A few seconds

Pulse V(t) calculation with circuit simulator

The proposed method makes several thousands of samples to be analyzable in just a day!

Analysis Tool for Logic/RTL Circuits



Problem

- Naïve method requires more than 1 week computation for a circuit with 100,000 gates
- Several Tens of thousands of samples are needed to achieve highly accurate estimation

Proposed Method

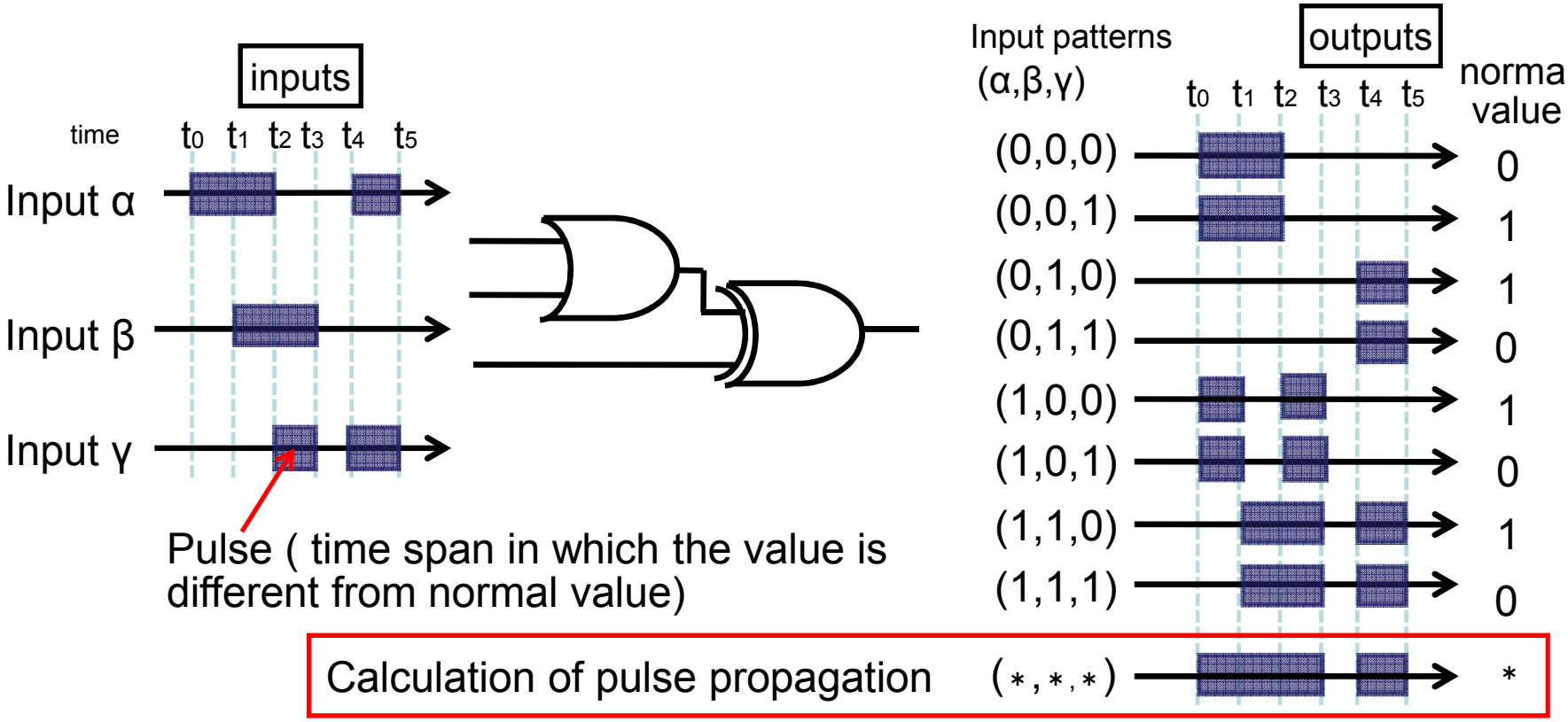
- Timing-aware fault simulation that ignores logical masking
- Logic-aware fault simulation that considers all the gates at a time
- Fault sequential simulation considering multiple faults

Computation in several hours for a circuit with 100,000 gates, guaranteeing the upper bound of error rate

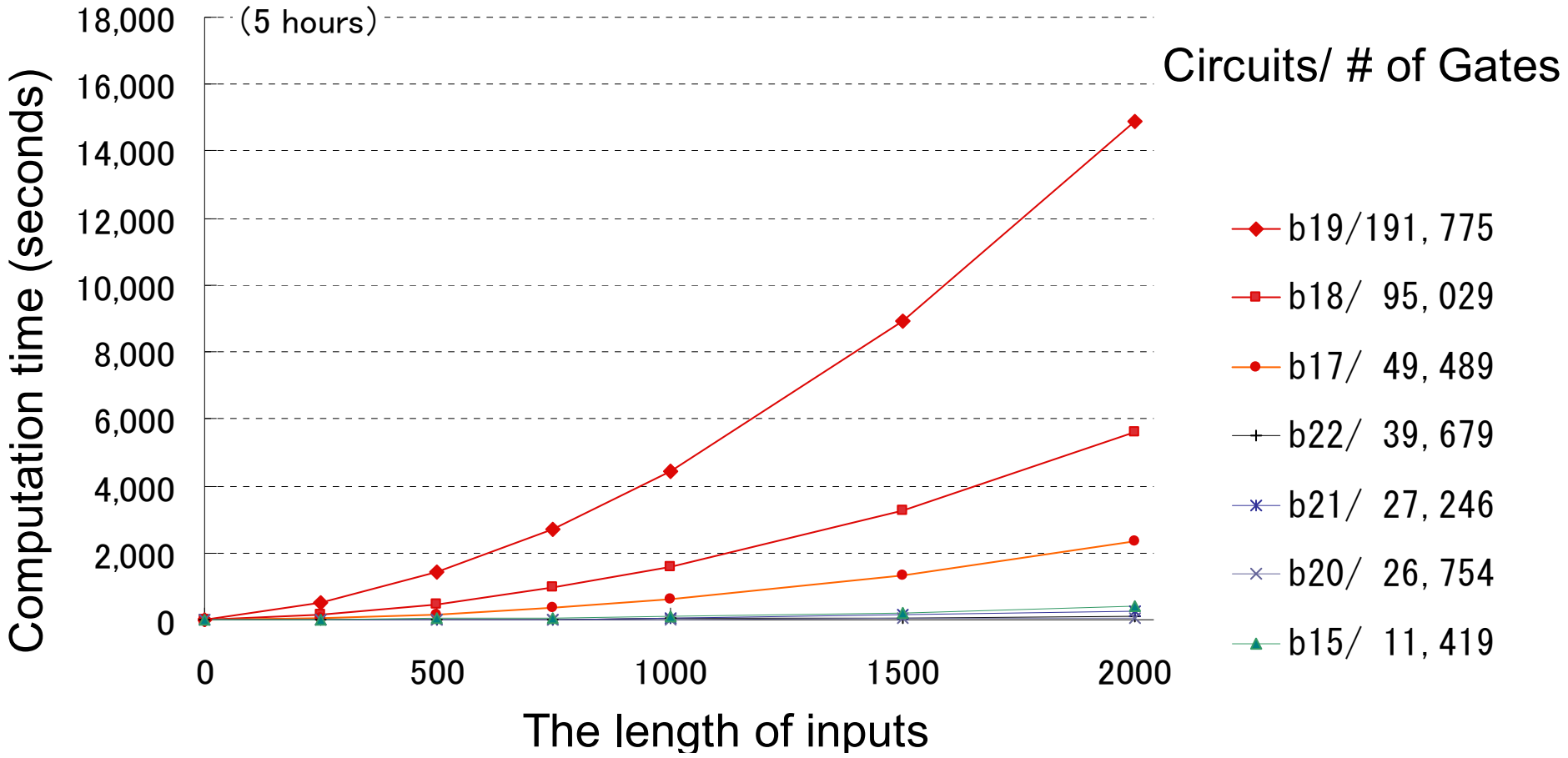
SEU : Single Event Upset
SET : Single Event Transient

Timing-Aware Fault Simulation

- Analysis of propagation of a pulse caused at a gate to flip flops and/or primary output terminals considering its pulse width and timing
- Calculate the upper bound of the pulse width and estimate probability of which the pulse is latched onto the flip flops
  - Consider the variation of pulse width on the propagation paths
  - Ignore effects of logical masking and re-convergence

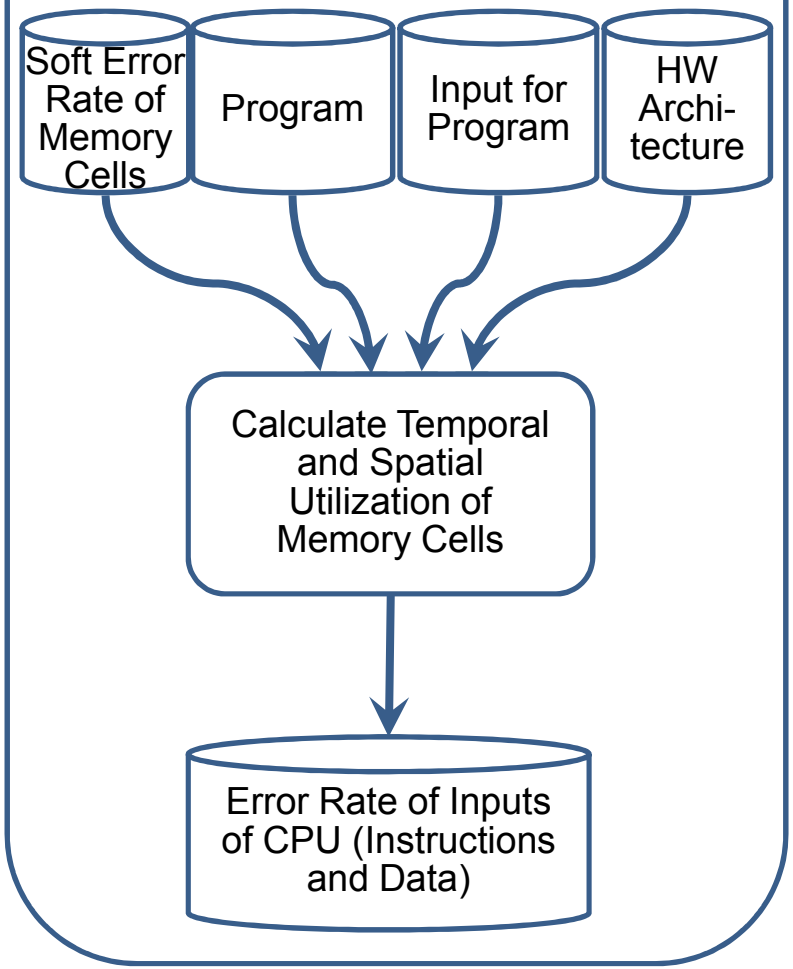


Computation Time of Accelerated Fault Simulation

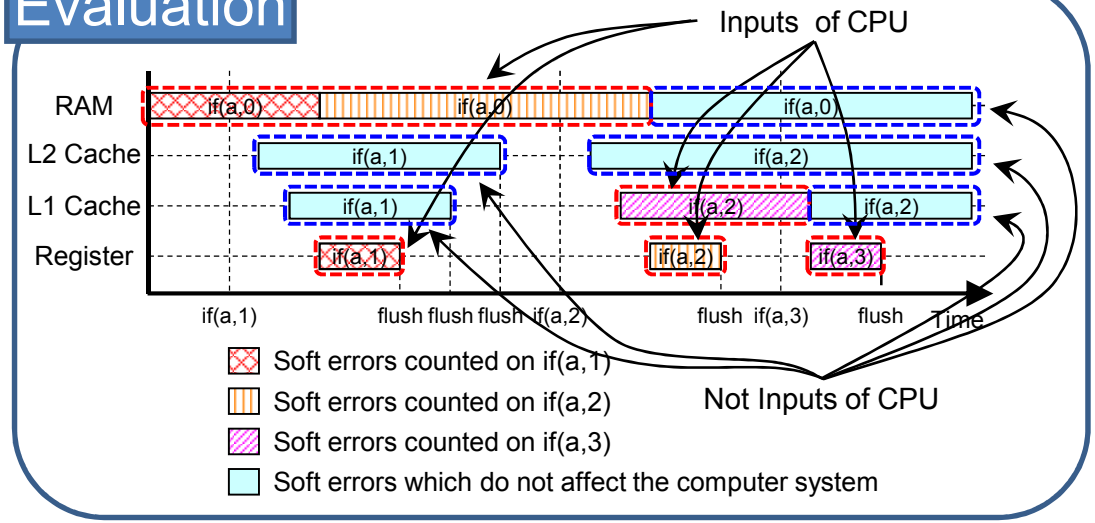


Memory System Simulator

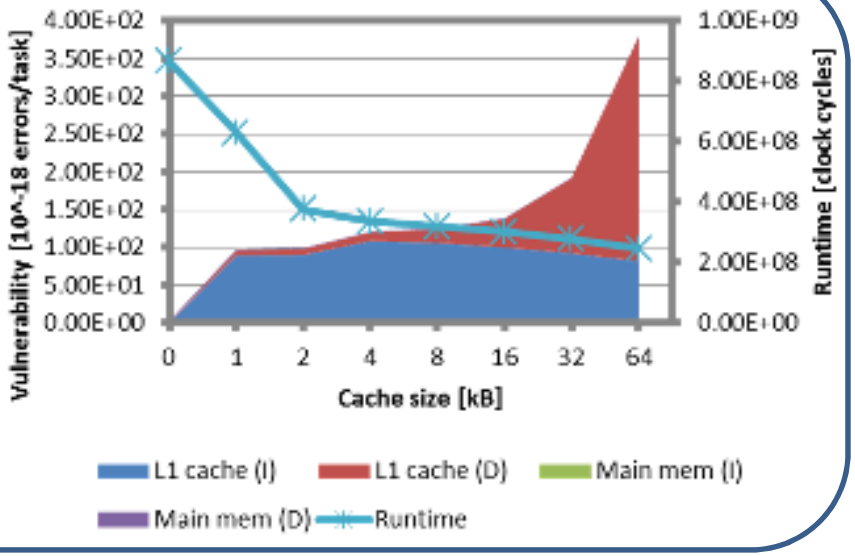
Analysis Flow



Evaluation



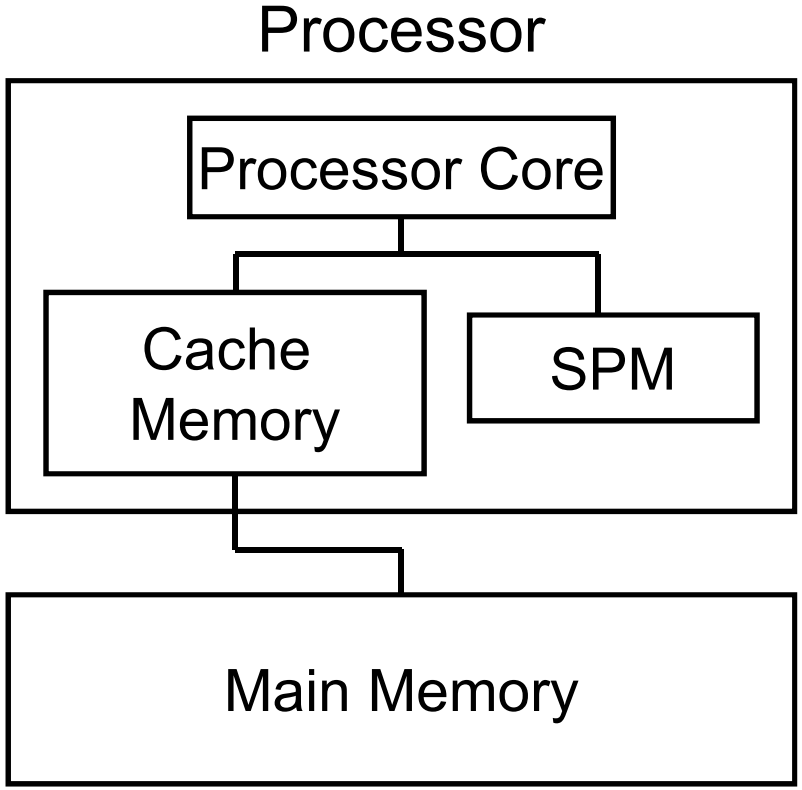
Results



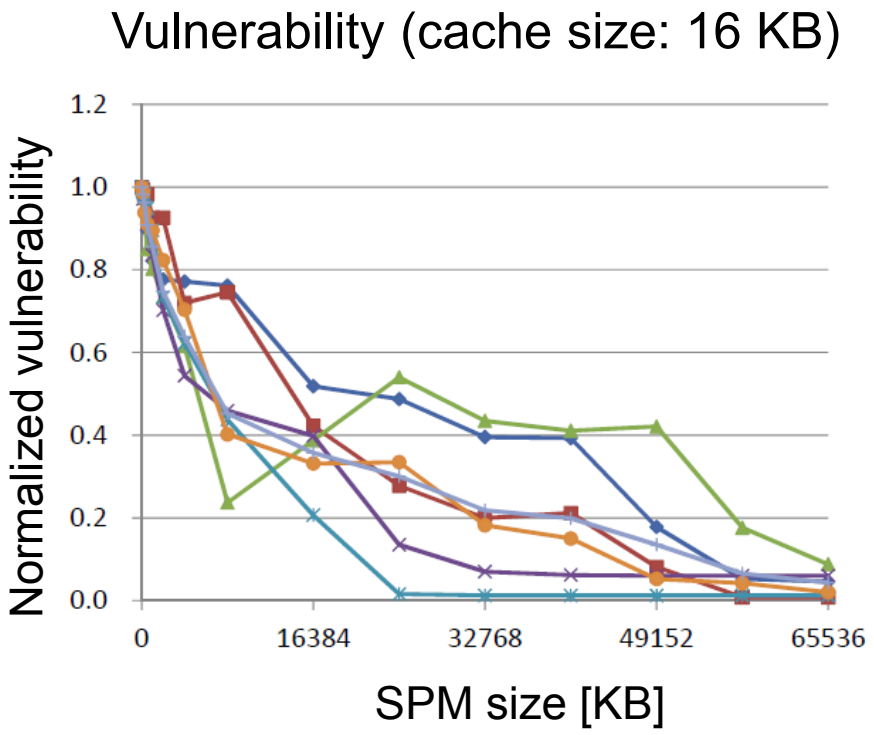
Example: Highly Dependable Design of Embedded Systems Using a Scratch Pad Memory

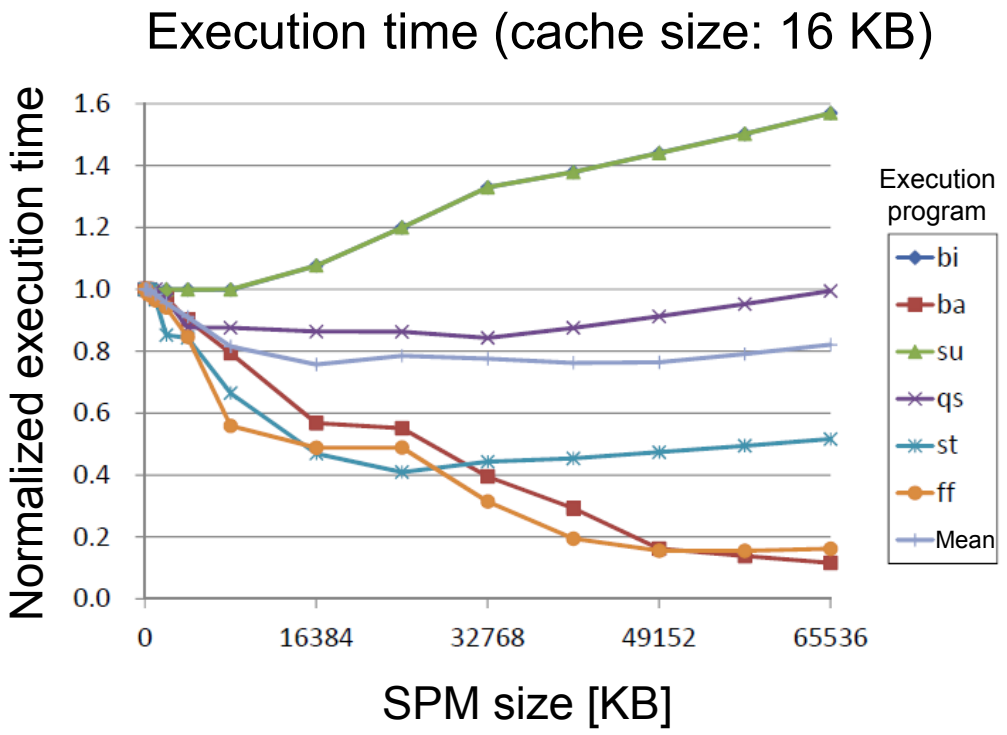
- No error correction in Cache Memory
- Error correction circuits in Scratch Pad Memory (SPM)

Improve dependability by allocation of program and data in SPM



Trade-off Analysis between SPM Size and Vulnerability (Inverse of Error Rate)





Summary

1. Concept of Design Flow and Tool Chain for Dependable VLSI
   - Unified tool chain from physical phenomena to system level for estimation of dependability compatible with hierarchical design flow
   - Three practical problems: Soft Error, Timing Error and Security
2. Soft Error Caused by Neutron
   - Analysis tools for logic cells, combinational circuits and sequential circuits (logic and register transfer levels)
   - Memory architecture simulator and trade-off analysis
3. Timing Errors by Fluctuation of Manufacturing
   - Introduction of Canary Flip Flops for reducing design margin
   - Improvement of static noise margin of SRAM
4. Design for Security
   - Trade-off analysis between testability and security