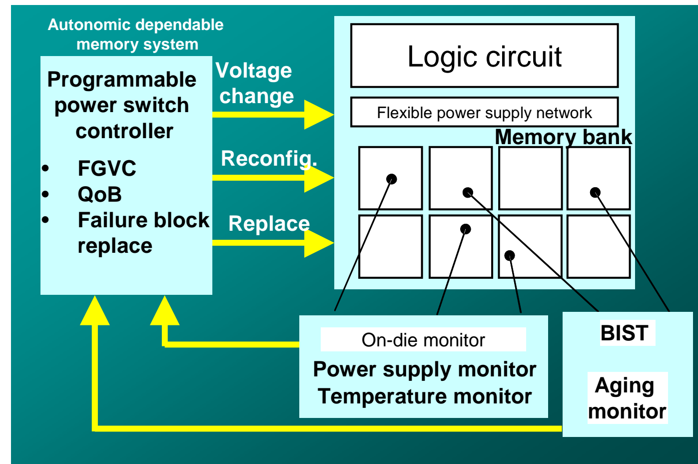
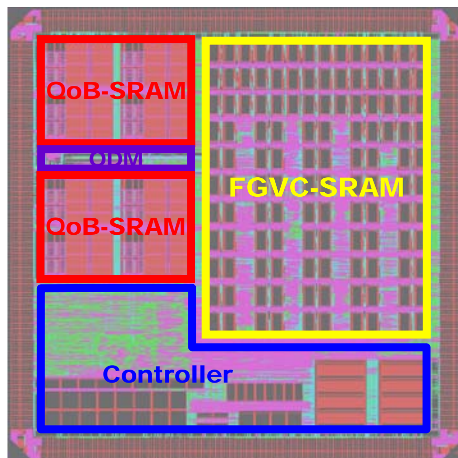
Dependable Memory Techniques for Highly Reliable VLSI System（Yoshimoto Lab. team）



BIST, ODM: Self-diagnosed circuits
FGVC(Fine Grain Voltage Control): Autonomic margin optimization
QoB(Quality of Bit): Autonomic change to 14T dependable mode

Autonomic dependable memory block diagram



Chip layout(40nm process, 5mm x 5mm)

●Research progress：

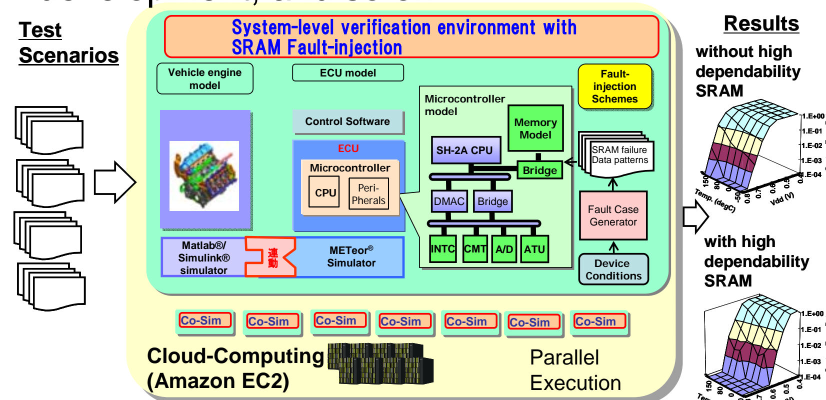
•Autonomic dependable memory system detects and avoids SRAM failure caused by Vth variation, aging, temperature fluctuation and power supply noise. The failure rate is improved 2-3 digit.

•Quality of Bit cell, fine grain voltage control scheme and power supply noise monitor are developed.

•System-level verification environment with SRAM fault-injection (Virtualization) is developed, and the improvement effects for ECU by proposed memory system are confirmed by virtualization.

●Future expectations：

•It is expected that each fundamental techniques, lockstep with QoB multicore and Virtualization technique are applied in LSI fabrication, system development, EDA development, and so on.



ECU fail rate evaluation by system-level verification environment (Virtualization)