Prof. Sakai's Team

- Formal Design Verifier: FLEC
  - Mathematically and automatically proves the correctness of logical designs
  - On a commercialization path with NEC and others
    - Has been applied to floating point cores utilized in various SoC for high-precision signal and financial computing
    - Regardless of bit-width (high-precision computing needs large numbers of bits), FLEC finishes within one second with 100% verification coverage whereas other EDA vendor tools take more than one year with only 1% verification coverage
- Timing-Fault-Tolerant Circuit/Architecture against Random Variation
  - Two-Phase Latch & Dynamic Timing Fault Detection enable Operation based on not Worst but Typical Case by Dynamically Balancing the Effective Delays among Stages
    - Max Freq is determined by Limit of Detection (2 cycles) ⇒ Twice of Existing Schemes
  - Architecture is Verified by Applying to an Out-of-Order Superscalar Processor
- Highly-Dependable FPGA : Highly-Dependable Use inc. Aerospace
  - Hard-Wired Triple Voters
  - User-Logic Reconfiguration Control Unit
    - Enables Self-Recovery from Any Fault on a Chip
- Dependable and high performance many-core architecture
  - Development of on-chip multifunction routers supporting ultra dependability
  - Development and verification of 180 FPGA prototyping system (on market soon)
    - With realistic configurations, our HW system emulating a many-core processor is 129x faster than the SW simulator
    - Development and evaluations of our task mapping method and the dependable mechanism for a many-nodes system