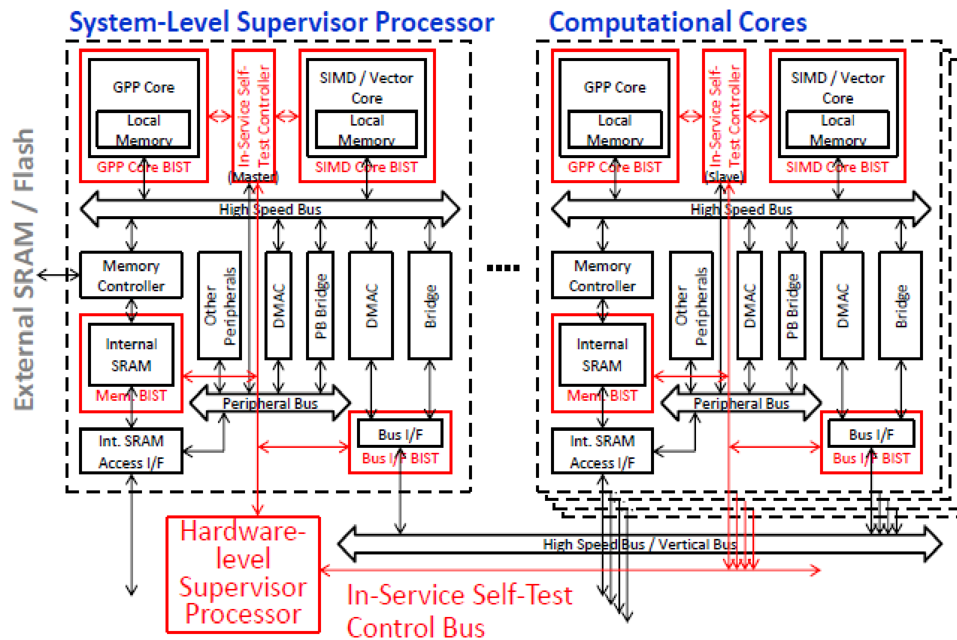
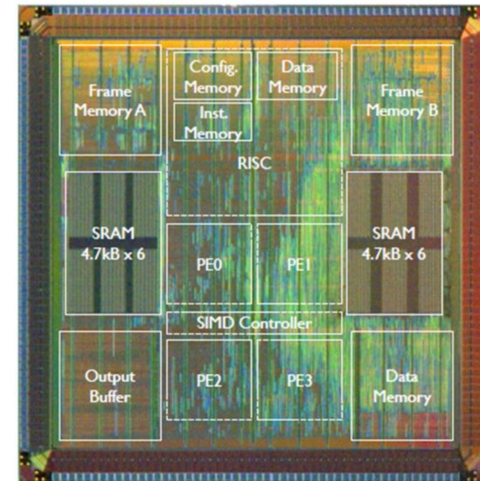
Development of Three-Dimensionally (3D) Stacked Graphics Processor for Automobile Application

System level design of 3D-stacked processor



Design, fabrication and evaluation of processor test chip used for optimizing 3D stacking technology



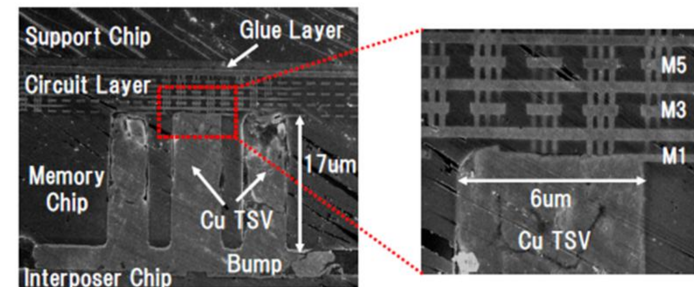
Chip specification:
Reconfiguration PE x 4
RISC controller x 1
Frame memory x 2
Output buffer x 1
Data memory x 1

0.13μm CMOS
1 poly/ 8 metal (Cu)
5mm x 5mm
980Kgates

Specification of 3D-stacked processor

System Configuration	4 stacked layers (1 SVP core＋3 PE cores)
Processor Configuration	SH-4A core+ on-chip memory (Chip size: 5mm × 5mm)
Bus Architecture (64bit)	Super Hyway bus (on-chip) Vertical bus with bus bridge (TSV)
Dependability Function	Self-test and self-repair by SVP, Multiplexed system control (Health data transmission by Heartbeat method), Self-test and self-repair built-in circuits (BIST, ScanPath, Majority circuit, TMR, BISR), TSVs with self-test and self-repair

SEM Cross-sectional view of 3D test chip with Cu-TSVs



TEG chip: 130nm technology node
TSV size: diameter 5μm, depth 15μm

*1: SVP (Supervisor Processor)
*2: TSV (Through Si Via)