Achieving Ultra Dependable VLSI

CREST-DVLSI
- Fundamental Technologies for Dependable VLSI Systems -

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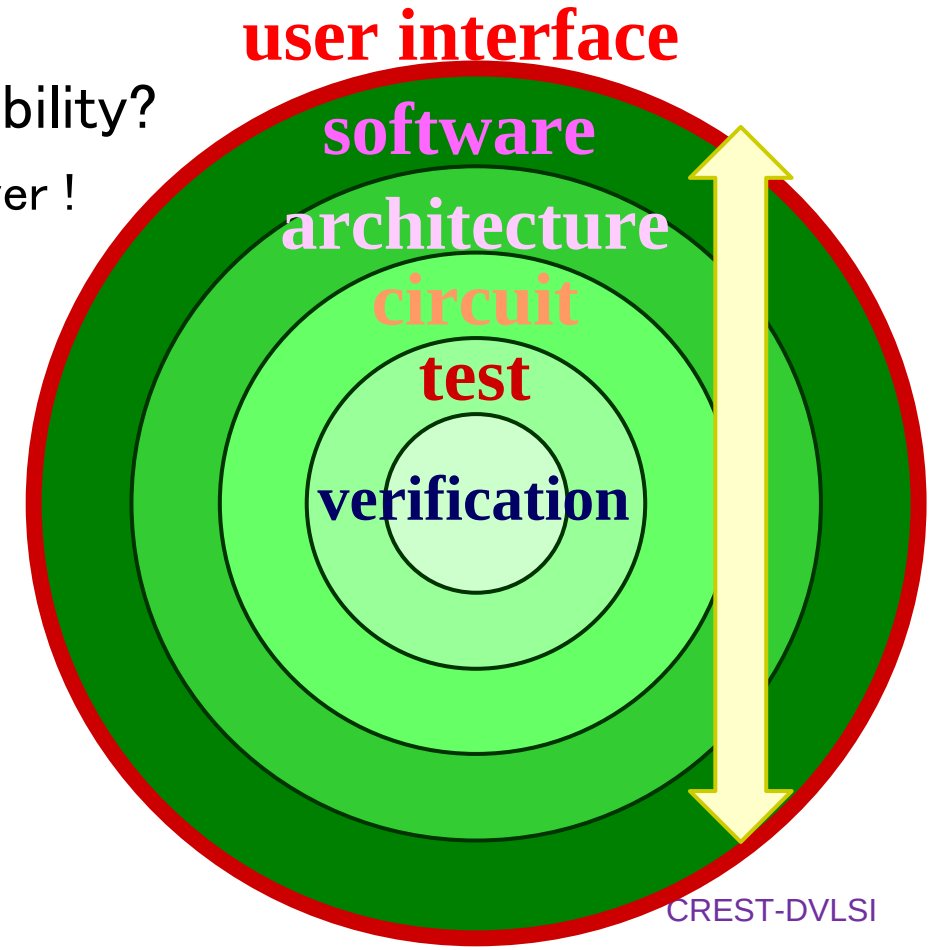
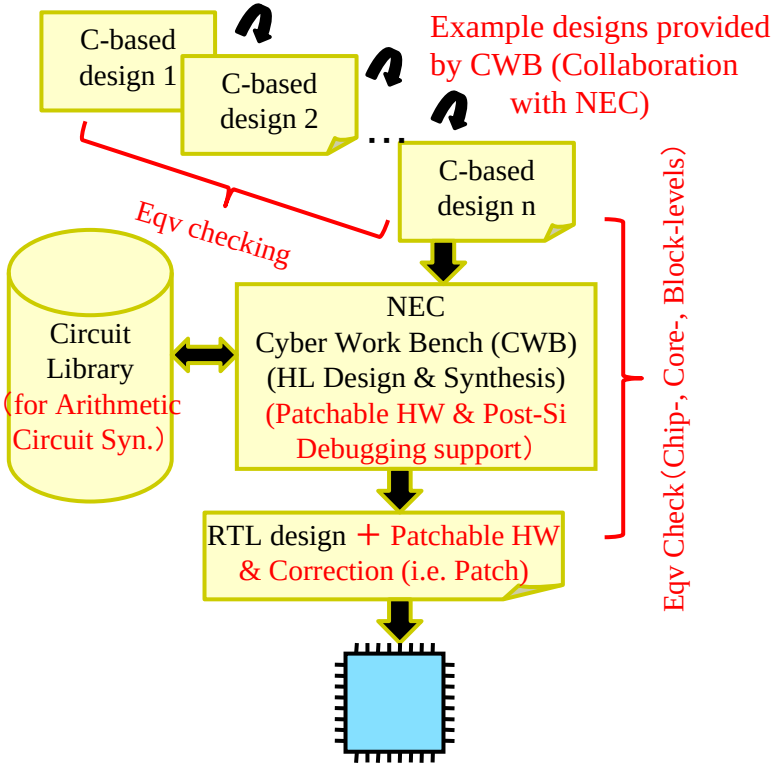
What is Dependability ?

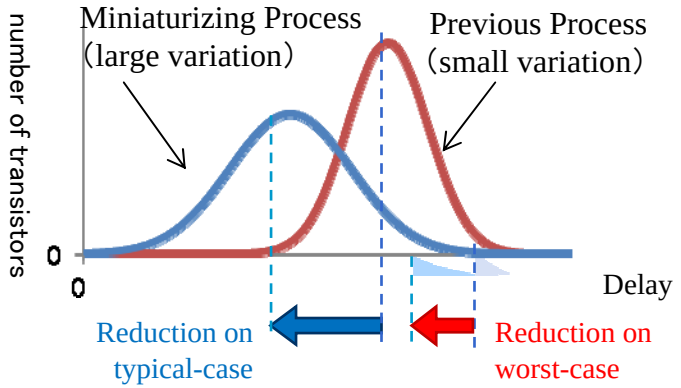
- Ring Model of Dependability
  - Where should dependability be defined ?
    - △ (~100% design) * (~100% hardware) * (~100% software)
    - ◎ only on user interface
  - What should we do for dependability?
    1. provide dependability in each layer !
    2. optimize among layers
       - complement each other
       - remove duplication
       - cost optimization
  - IEC61508 / ISO26262
    - functional safety (dependability)
    - deterministic / probablistic



New Design Balance

- Formal Verification vs Simulations
  - Fujita's Research
    -> large scale verificaiton
  - Wakabayashi's Research
    -> output to the real world!
- Worst Case Design vs Best Effort Design
  - Sakai-Goshima's Research
    -> Best Effort Design!
  - Kise's Research
- Fault Tolerant Many Core

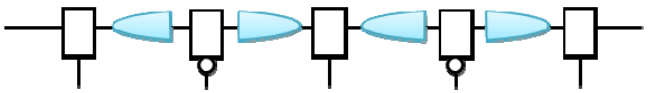


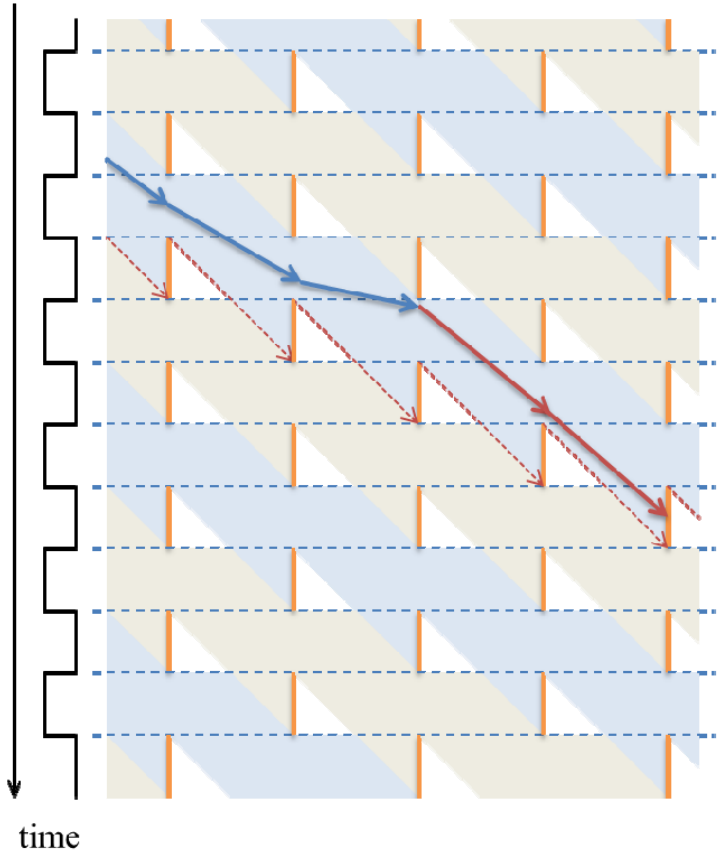


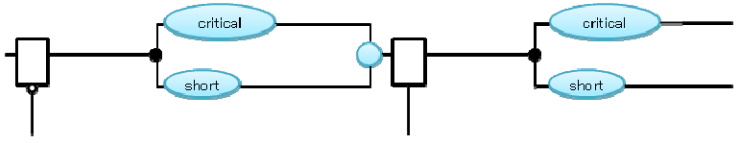
Best Effort Design and Run Time Recovery

- Complexity / Variation
  - gigantic design cost
- Best Effort Design
  - design in nominal case
- Run Time Recovery
  - Faults, detect them all !
  - recover by architecture / software
- Ensuring User Level Dependability
  - prevent errors
  - preserve time constraints

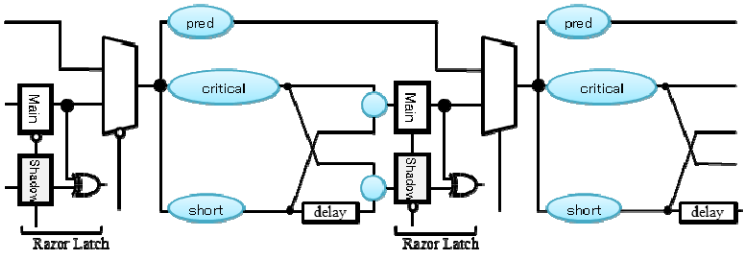
e.g. Time Borrowing + Recovery



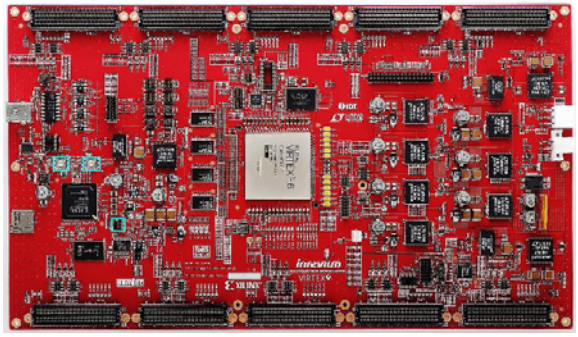


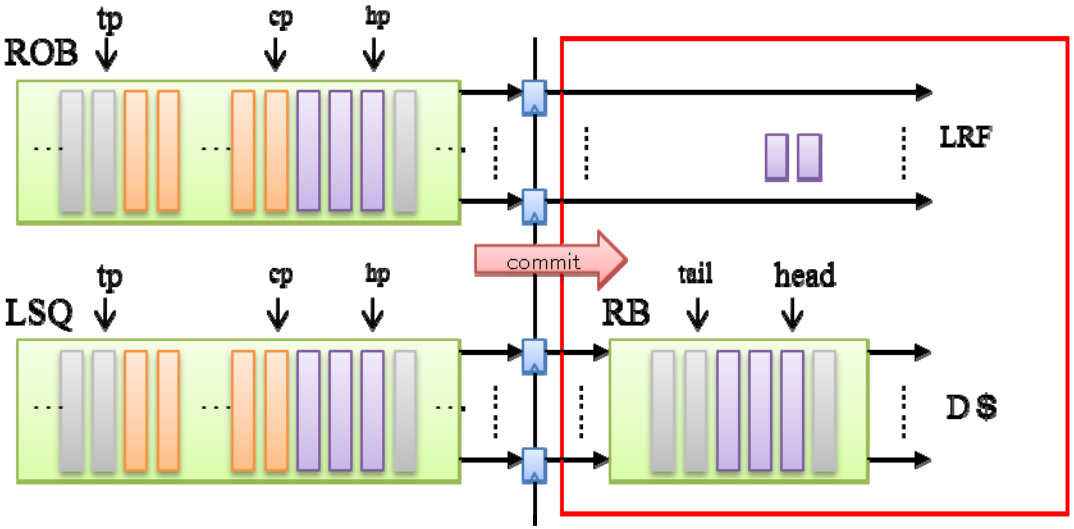


2-phase latch



Proposal





Questions

1. Are the followings true?
   - VLSI design miss / sotware bug = deterministic
   - soft error, hard error = probablistic
2. Software is a product of best effort …
   - why not design?
   - why not circuits?
3. Who cares the design balance among layers?
   - horizontal distribution of works
   - packaged design of architecture and software
4. What is the most important thing?
   - industry
   - university
   - users (society)