Tunnel Transistor

Tunnel Field-Effect Transistor (FET) using III-V/Si Heterojunctions

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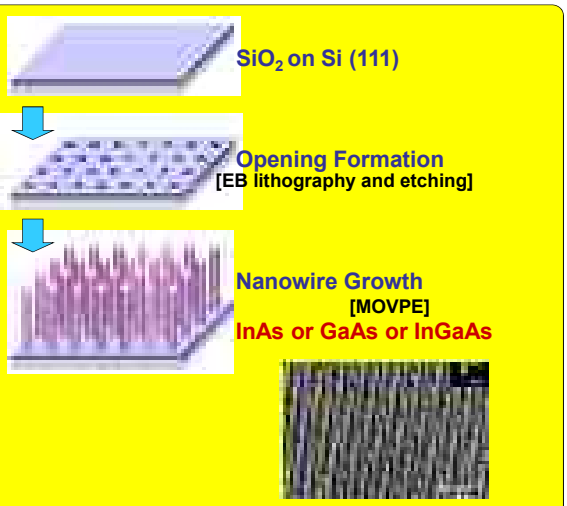
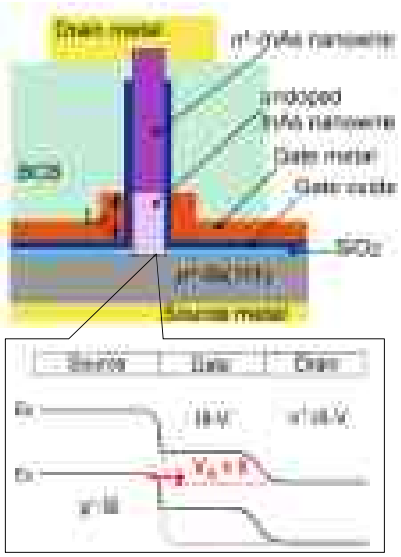
1.Introduction

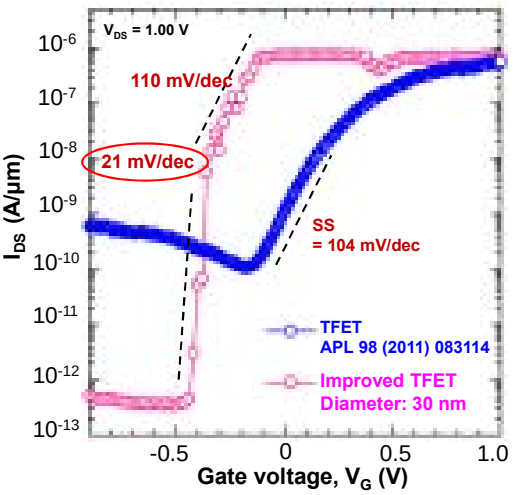
Conventinal MOSFETs have theoretical limit in subthreshold slope(SS) characteristics resulted from carrier diffusion (SS > 60mV/dec.). Our technology can realize steep-slope nanowire-based FET by controlling III-V/Si heterojunctions without misfit dislocations, which can be achieved with nano-heteroepitaxial methods.

2. Device Structure, Performance of the Tunnel FET



III-V/Si Heterojunctions Growth Process



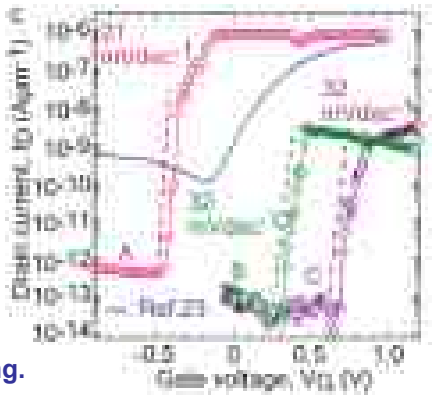


-The combination of a narrow band gap III-V with Si is a good system for boosting up the ON-state current and has high band-to-band tunneling efficiency.
-The subthreshold slope(SS) is far lower value than 60mV/dec.(theoretical limit value) of Si FET.

3. Synthesis of Nanowire by using Pulse Doping

With respect to the impurity density of undoped InAs nanowire, supply the p-type dopant of the $10^{16}cm^{-3}$ to compensate for the n-type dopant once for x seconds, to make the electrically neutral intrinsic layer.

Growth Process of Nanowire



InAs/Si Tunnel FET

-The turn-on voltage can be adjusted by the supply time of dopant in pulse doping.
-The leakage power in a standby state can be further reduced.

4. Application Examples

-Low voltage operation transistor
-Low power consumption LSI
-Sensing devices for IoT

5. Patent Licensing Available

Patent No.: WO2011/040012, WO2015/022777 (US2016/0204224, JP, EP, CN, KR, TW)
WO2015/064094 (US2016/0284536, JP, EP, CN, KR, TW)

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