Electronic Device

Semiconductor Structure provided with AlON Film on top of Ge Layer

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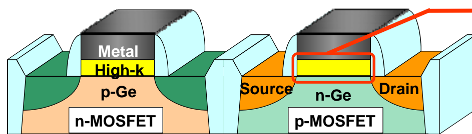
1. Abstract

- By forming aluminum oxynitride on the Ge (Germanium) layer, high reliability thin film as the gate insulating film of MOSFET was realized.
- High-pressure inert gas post deposition annealing (PDA) using N_2 or Ar gas dramatically improved the electrical properties of AlON/Ge MIS gate stacks.

2. Ge MOSFET: Expectation, and Problems to be Solved

- Ge which has the higher carrier mobility, is a promising candidate as a channel material in the next generation of MOSFETs.
- In miniaturized MOSFETs, gate insulators with a high dielectric constant (high-k) are required in order to suppress the gate leakage current and the short channel effects.
- There is also a problem how good interface and insulating layer on Ge can be realized.



Ge MOS FET Structure

Gate Stack
Ge-insulation film interface
GeO_2 -High-k Interface
Problems:
- Degrade carrier mobility
- Less reliability
- Variation increase

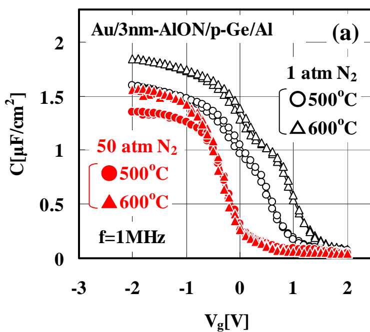
3. Scalable High-k/Ge Gate Stack Technology

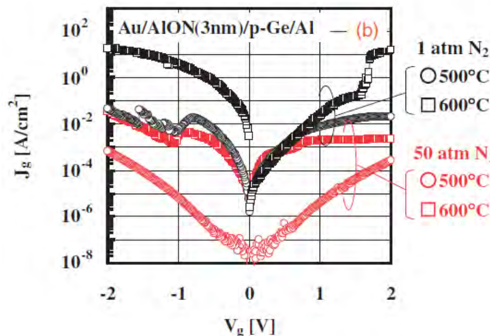
High-pressure N_2(HPN) (or Inert Gas) heat treatment

AlON / Ge → AlON / Ge → AlON / GeON / Ge

- We investigated the use of aluminum oxynitride film (AlON) as a gate insulating film formed on the Ge substrate. By using an AlON film, a thin EOT (Equivalent Oxide Thickness) is possible.
- However, heat treatment of AlON film in order to improve the quality of the AlON film deteriorates the interface between Ge substrate and the AlON film.
- After examining the conditions under which the interface between the AlON film and the Ge substrate is not degraded by heat treatment, we tried to apply high-pressure N_2 post-deposition annealing (HPN PDA) in order to suppress the N_2 desorption, which was analogous to high-pressure oxidation (HPO) annealing in GeO_2/Ge stack.

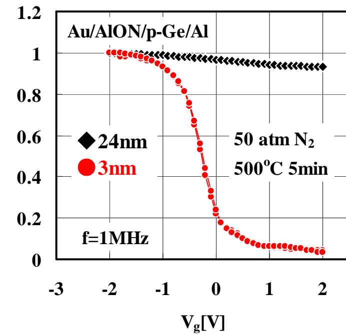
- HPN PDA dramatically improves the C-V characteristics, whereas the large interface states were observed in the same gate stack as a result of atmospheric-pressure N_2 (APN) post-deposition annealing.
- HPN PDA also reduces the gate leakage current.
- HPN PDA only improves the interface in the case of thin AlON/Ge.





C-V Characteristics (a) and I-V Characteristics (b)

Au/3nm-thick AlON/p-Ge(100)/Al MIS capacitors in APN and HPN PDA at 500 and 600 degree.



C-V Characteristics

Au/3nm-thick and 24nm-thick AlON/p-Ge(100)/Al MIS capacitors in HPN PDA at 500degree for 5min.

Patent Licensing Available

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