Electronic Device

Energy Efficient Power Gating Architecture using NV-SRAM & NV-FF

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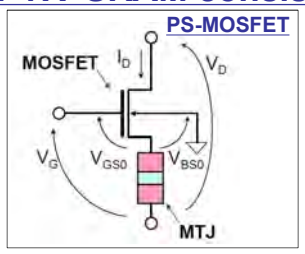
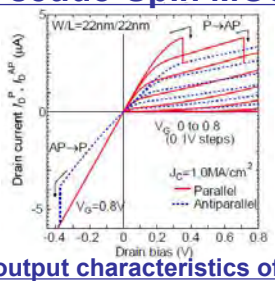
1. Abstract

- A new power-gating architecture using non-volatile SRAM (NV-SRAM) and non-volatile FF (NV-FF) circuits, called non-volatile power-gating(NVPG), was developed.
- Pseudo-Spin metal-oxide-semiconductor field effect transistors (PS-MOSFETs) are used in the non-volatile bi-stable memory circuits.
- The proposed NVPG architecture can dramatically reduce the energy issues caused by static power dissipation in advanced CMOS logic systems.

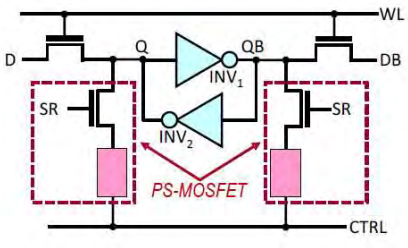
2. NV-SRAM consisting of Pseudo-Spin MOSFET



Circuit configuration



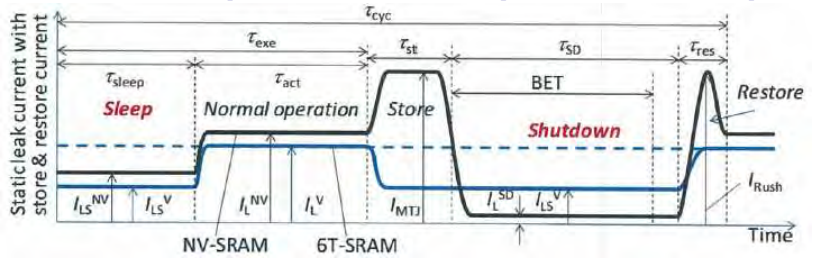
Simulated output characteristics of the PS-MOSFET



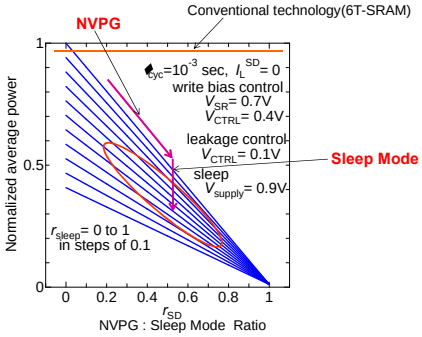
NV-SRAM cell

- The spin-transfer torque magnetic tunnel junction (MTJ) is connected to the source of the MOSFET.
- The MTJ feeds back its voltage drop to the gate, and the degree of negative feedback depends on the resistance state of the MTJ.
- In these NV-SRAM cell circuits, the MTJs can be electrically separated from the inverter loops by the PS-MOSFETs and thus have no degradation effects to fundamental circuits of the inverter loops.

3. NV-SRAM operation for low power consumption

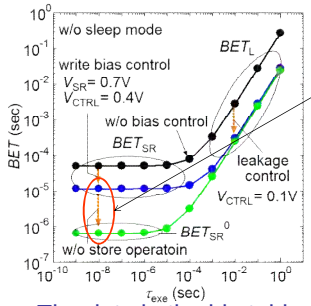


Low power operation of NV-SRAM combining with NVPG and Sleep mode



- BET (Break-Even Time): Power-shutdown time to compensate for the extra energy required to provide power gating.
- The standby power of NVPG is less than 50% of the conventional technology.
- By introducing a sleep mode, power consumption can be further reduced more than 50%.

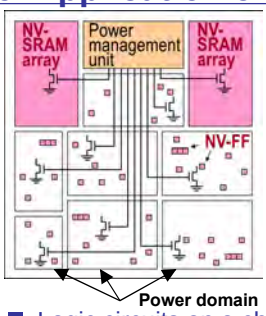
4. BET reduction architecture



BET is greatly reduced
➔ In the result, the energy reduction efficiency is further improved.

- The data in the bi-stable circuit is not stored in the NV-memory element (MTJ) when the data in the bi-stable circuit and the data in the NV-memory elements match.
  - ➔ This architecture which reduces the number of write into MTJ makes BET greatly reduced.
  - ➔ The energy consumption is also greatly reduced.

5. Application examples



Schematic of NVPG processor/SoC using NV-SRAM and NV-FF

- Logic circuits on a chip are partitioned into several circuitry domains. (power domains)
- The power domains are electrically separated from power-supply lines and/or ground lines by sleep transistors.
- These domains can be shut down during standby mode without losing their data by using NV-SRAM and NV-FF, and thereby highly energy-efficient power-gating can be achieved.
  - ➔The static power is considerably reduced even during system run-time.

Patent Licensing Available

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