Green Computing and DX

R&D Project Title : Multilane and Multilevel Pipelined Coarse-Grained Reconfigurable Linear Array

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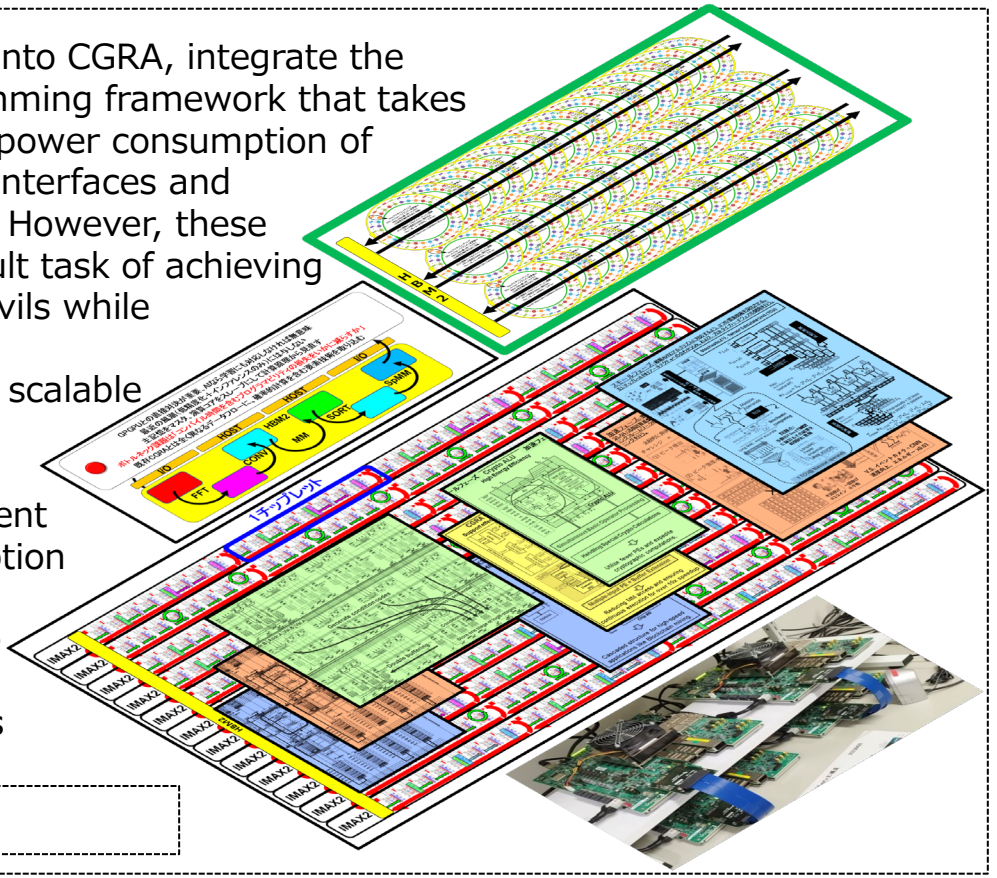
R&D Team : None

Summary : We merge three types of calculation platforms into CGRA, integrate the calculation mechanism and data flow, and develop a programming framework that takes advantage of its high-speed compilation characteristics. The power consumption of traditional computing infrastructure is due to fancy memory interfaces and high-frequency memory traffic to support high performance. However, these are also necessary evils for maintaining versatility. The difficult task of achieving 100 times more energy efficiency by eliminating necessary evils while maintaining a certain level of versatility work.

① Ultra-compact stochastic digital CGRA for sensor layers: A scalable stochastic calculation mechanism that combines spike coding and snapshots. Tops/W:1000 times better than GPU.

② Digital-only CGRA for next-generation security: Development of general-purpose CGRA for various hash calculation/encryption /decryption algorithms. Tops/W:300 times better than GPU.

③ Large-scale digital general-purpose CGRA for intermediate and final layers: Development of a macro pipeline CGRA that connects IMAX2 (general-purpose CGRA). Tops/W:100 times better than GPU.



http://archlab.naist.jp